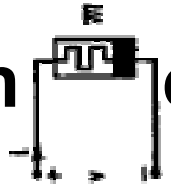
SAND2011-1188C

Neuromorphic Computing with  emristors

February 24, 2011

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Albuquerque, NM, 87185

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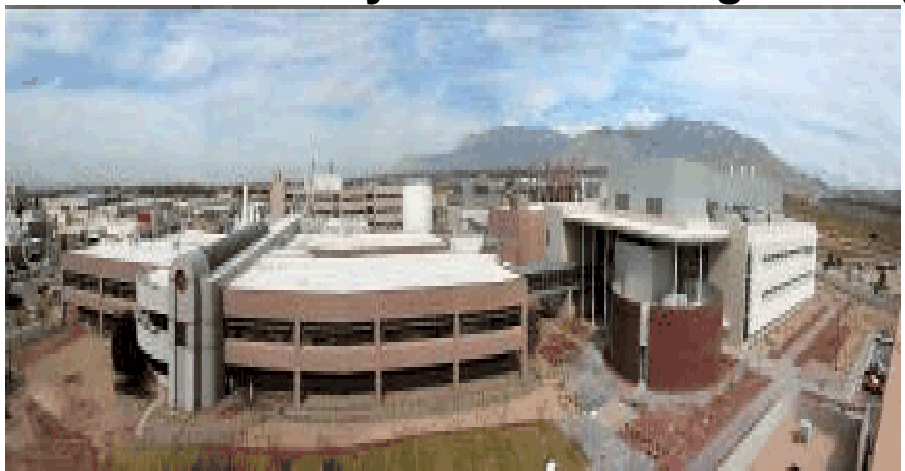
Outline

- Introduction
  - About Me and Sandia
  - Background/Goals
- All About Memristors
  - How Does the Memristor Work?
  - Memristor Models
  - Sandia's First Memristors
- Hardware Based Neuromorphic Computing
  - Intro
  - Low Level: Spike-timing-dependent plasticity
  - Intermediate: Memron
  - Higher Level: Cog ex Machina
- Summary and Future Work

Part I: Background

About Me and Sandia

- My background is Electrical Engineering
  - Specialize in Semiconductor Device Physics
- My work: Advanced semiconductor device research
- Leading memristor effort at SNL
- Center I Work For: MESA (1700)
- Microsystems and Engineering Sciences Applications
  - Largest single Federal investment in microtechnology
  - $462M capital line item; completed in 2008
  - 391,000 square feet of fab, lab, and office space
- Useful to create any hardware imaginable (including neuromorphic)



U.S. DEPARTMENT OF ENERGY

National Nuclear Security Administration

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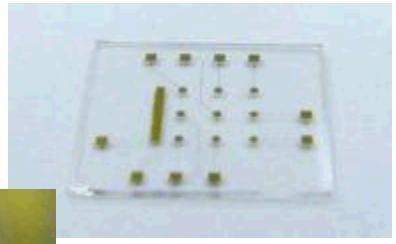
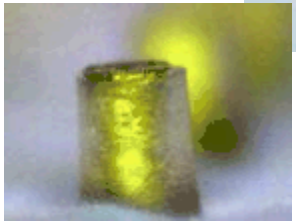
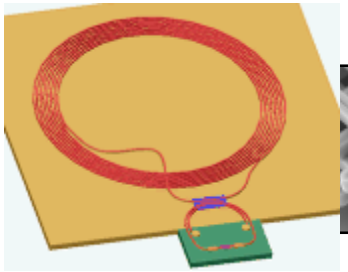
MESA Complex

Enabling Microfabrication Technologies

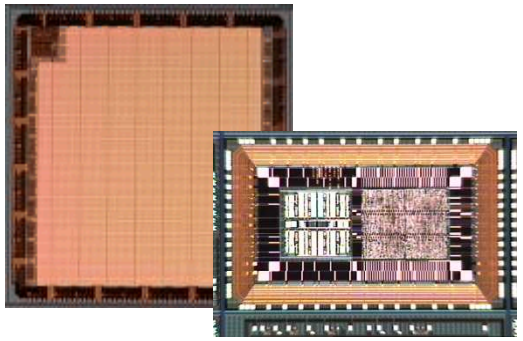




Flexible Fabrication

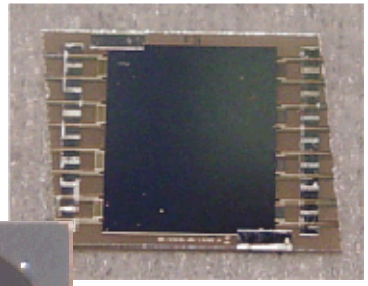


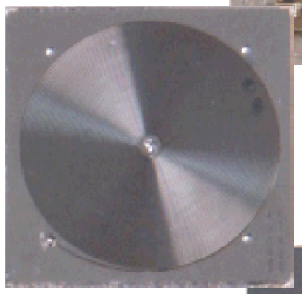
Photonics



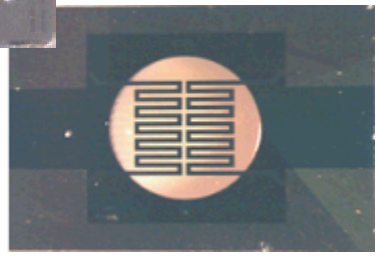
Si CMOS

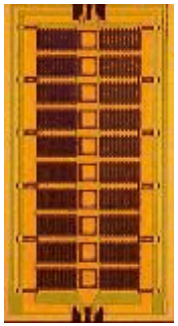
Piezoelectrics



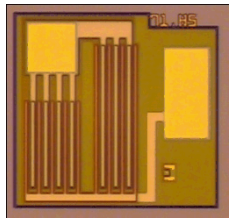


Si Bulk Micromachining





3.6mm

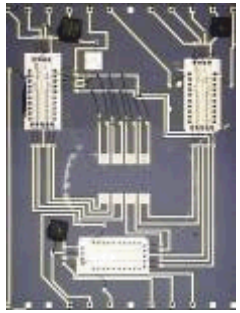


1.8mm

HBT Compound Semiconductors

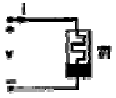
Neuromorphic Hardware ????

Advanced Packaging



Background

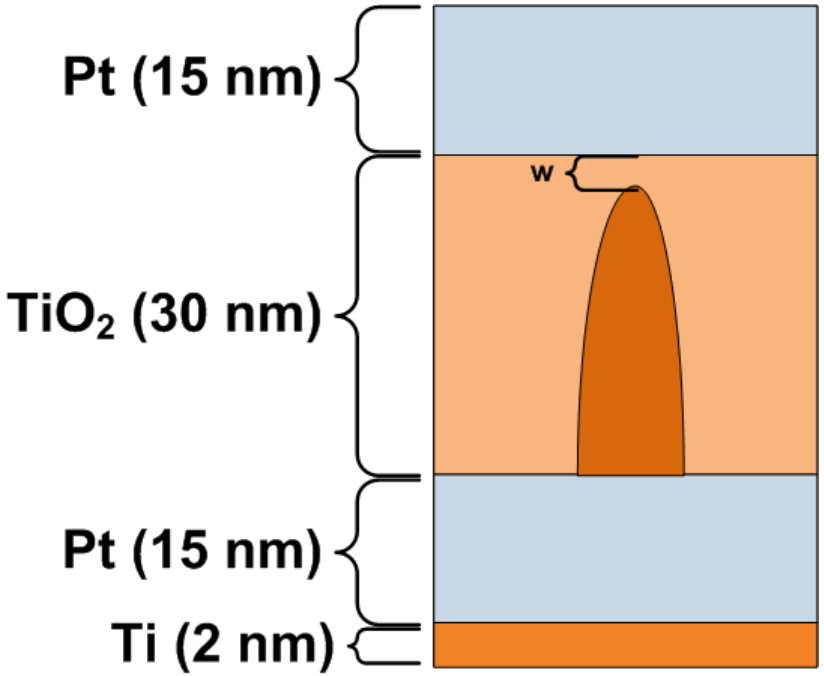
- I began general memristor research in mid/late 2010
- Cognitive science staff began investigating memristors for use in neuromorphic systems in early/mid 2010
- Collaboration was born late last year
- Main Goal: Demonstrate memristor based neuromorphic systems in hardware
- Investigating multiple ways to do this:
  - Analog: Mimic biology (different ways to do this)
  - Digital: Use memristive memory to achieve the same results
- Applications
  - Low power supercomputing
  - End of Moore's law architectures
  - Pattern recognition

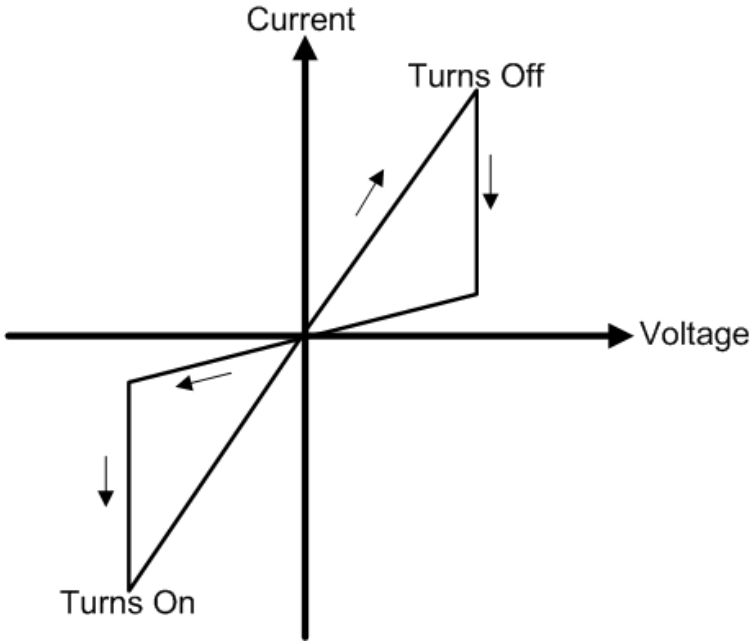


Part II: Memristors

What is a Memristor?

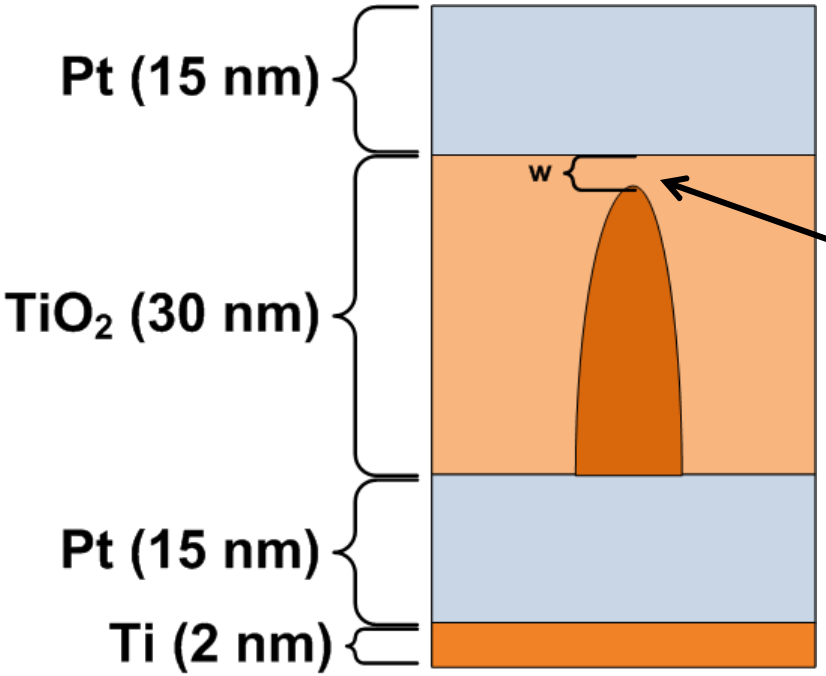
- Memory + resistor = Memristor
- A semiconductor resistor that remembers its state
- Information is stored as the position of a nanoscopic set of ions
- w = state variable



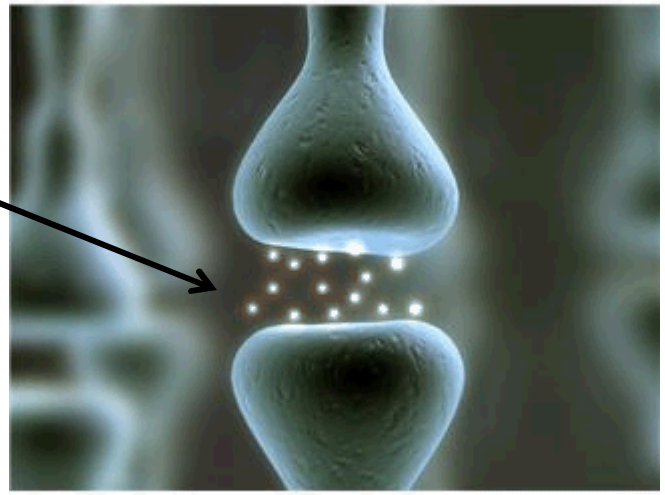


Why do Neuroscientists Care?

- In short, the memristor is an electrical synapse
- Synaptic weight = memristor state
- I hope to elucidate this point during this talk



memory



wikipedia.org

More Detailed Definition

- At this point, the definition of "memristor" is twofold:

1. A true memristor is a *theoretical device*
   - Leon Chua proposed concept in 1971
   - Chua and his student Kang generalized as "memristive systems" in 1976
   - Mainly a mathematical/EE novelty from 1976 to ~2008
2. Since 2008, the word "memristor" is used to describe two terminal memristive devices
   - Memristive semiconductor devices have been observed numerous times since 1962…
   - Hickmott – Voltage Controlled Neg Resistance (1962)
   - Kozicki – PMC memory (1995)
   - Samsung – NiO res switching (2005)
   - HP –first to use term *memristor* to describe real device (08)

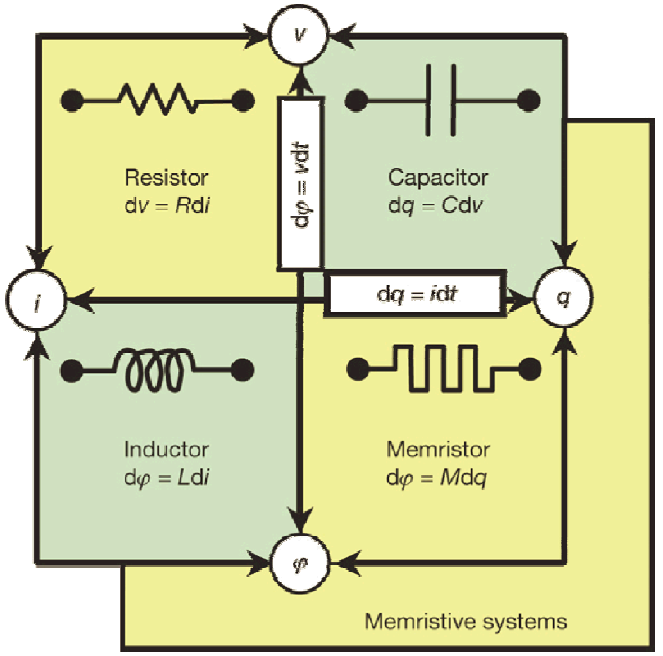
What is Memristor – in Theory?

- Theoretical concept created by Leon Chua in 1971
- 4th passive element "necessary for the sake of completeness"
- Chua suggests building a q-φ curve tracer* to characterize
- Charge controlled and flux controlled
- Two state eqns (*w* = state variable):

Leon Chua, father of the memristor

$$v=R(w,i)i$$

$$dw/dt=f(w,i)$$

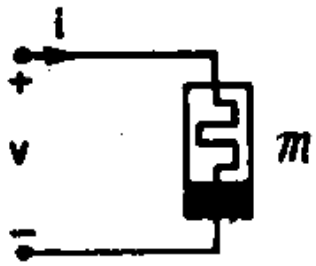


Strukov et al, Nature 459, 1154, 2009.

*Chua does give a schematic for a q-φ curve tracer in the original paper

EE Definition of a Memristor

- **Any electrical engineers in the audience?**



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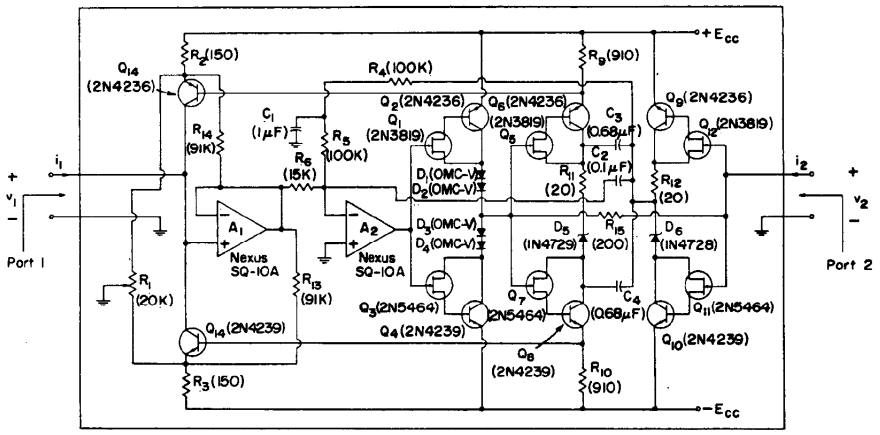
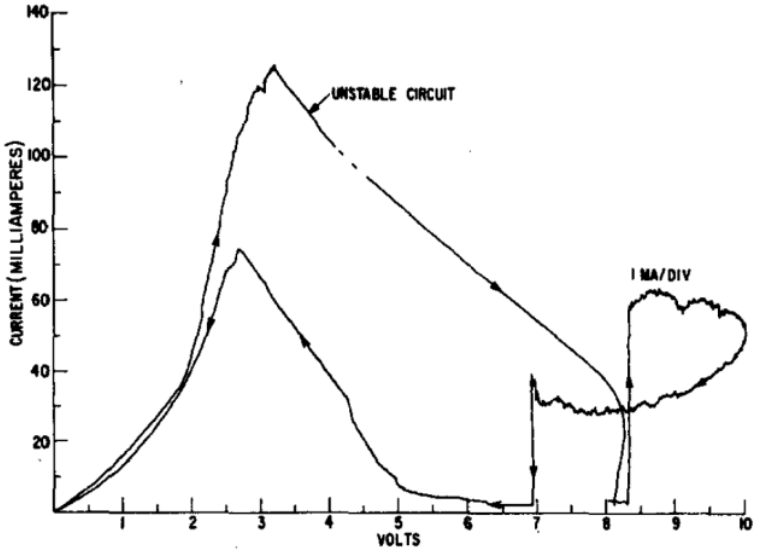


Fig. 2. Practical active circuit realization of type-1 M–R mutator based on realization 1 of Table I.

L.O. Chua, IEEE Trans Circuit Theory 18, 507, 1971.

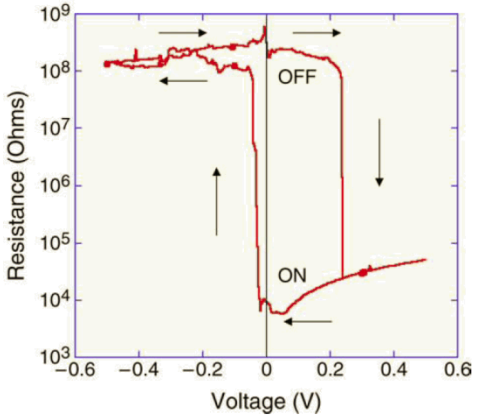
History of Memristive Devices

Al_2O_3 MIM Cap (in 1962)
Voltage Controlled Negative Resistance



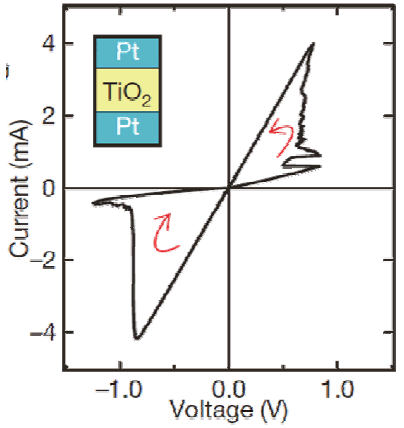
T.W. Hickmott, J. Appl. Phys. 33, 2669, 1962.

PCM, Patented by Kozicki in 1998:
Chalcogenide/Ag MIM Cap



Kozicki et al, Supperlattices and Microstructures 34, 459, 2003.

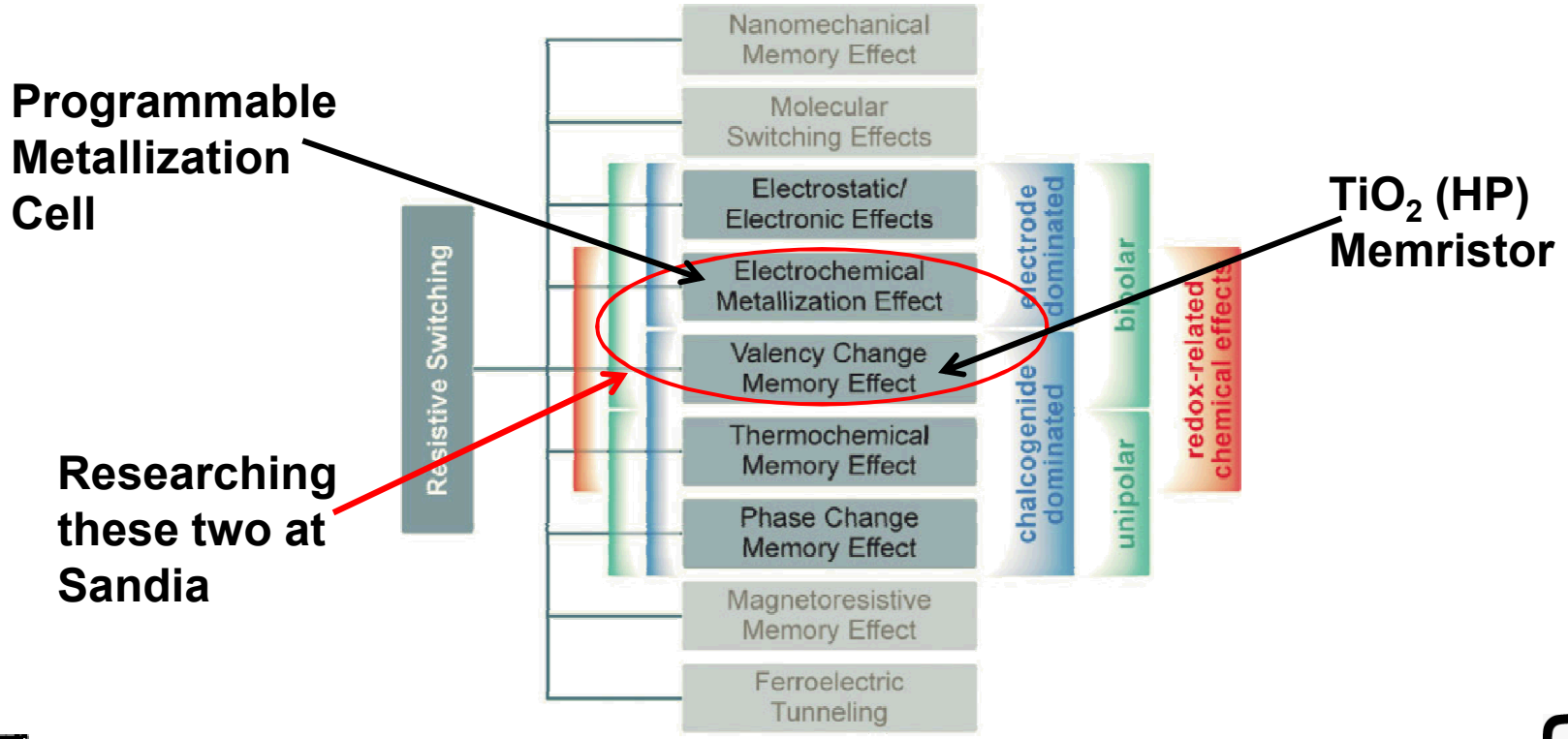
TiO_2 MIM Cap:
HP Labs' "Memristor"



Strukov et al, Nature 459, 1154, 2009.

Real Memristors

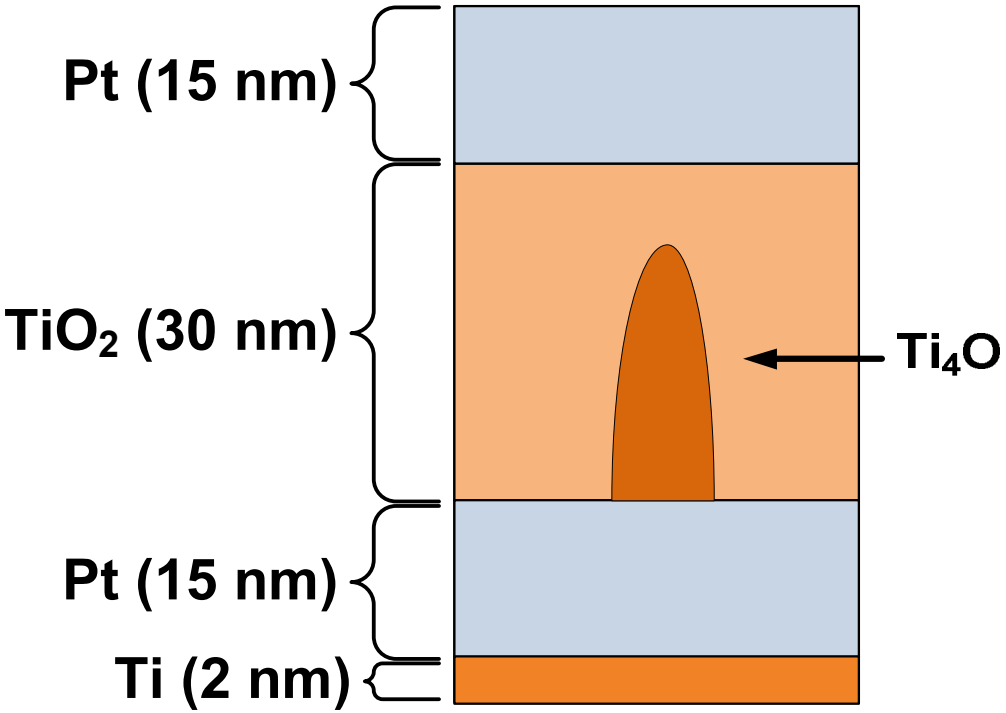
- The device that HP and others call a memristor is really a memristive device and a form of Resistive or Redox memory
- Redox memory is a leading contender for flash replacement
- Several types of Redox memory, categorized by Wasser:



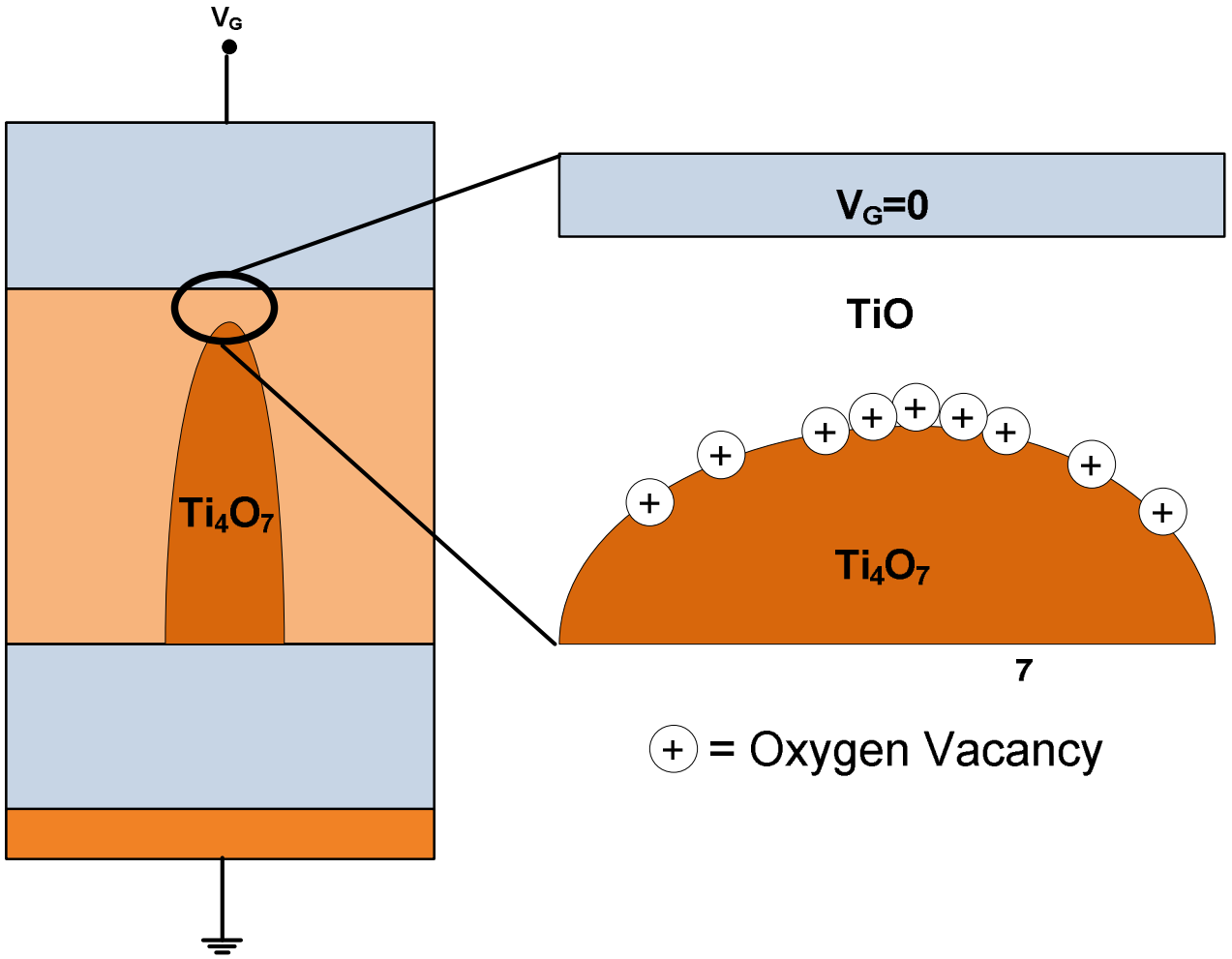
R Wasser et al, Adv Mat 21, 2632, 2009.

How Does the TiO_2 Memristor Work?

- First step: Electroforming
- Apply high voltage to create a conducting filament through the insulator



How Does the TiO_2 Memristor Work?



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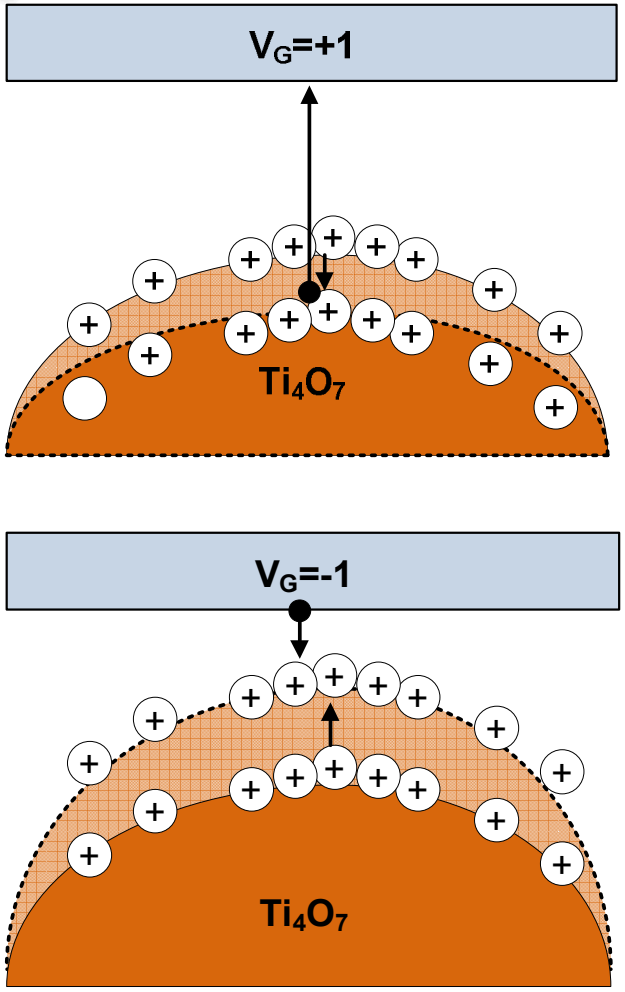
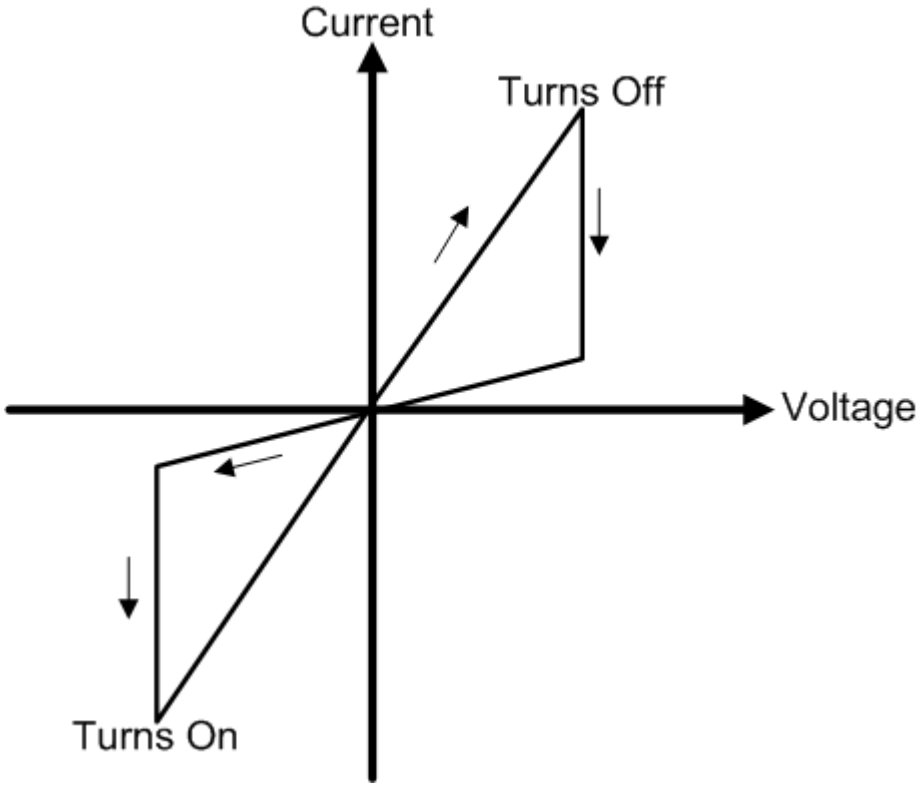
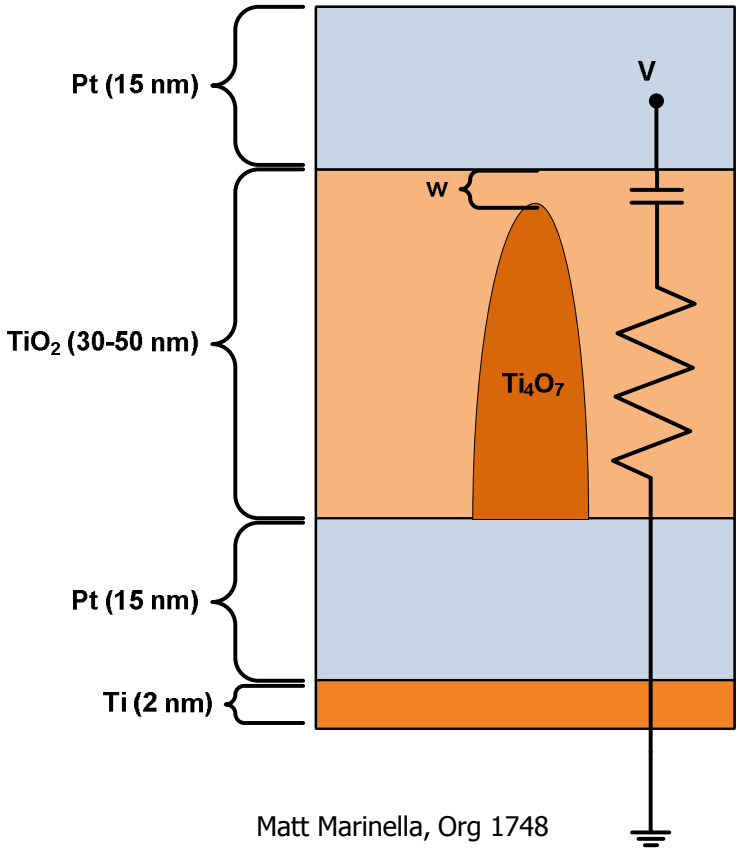




HP Memristor Model

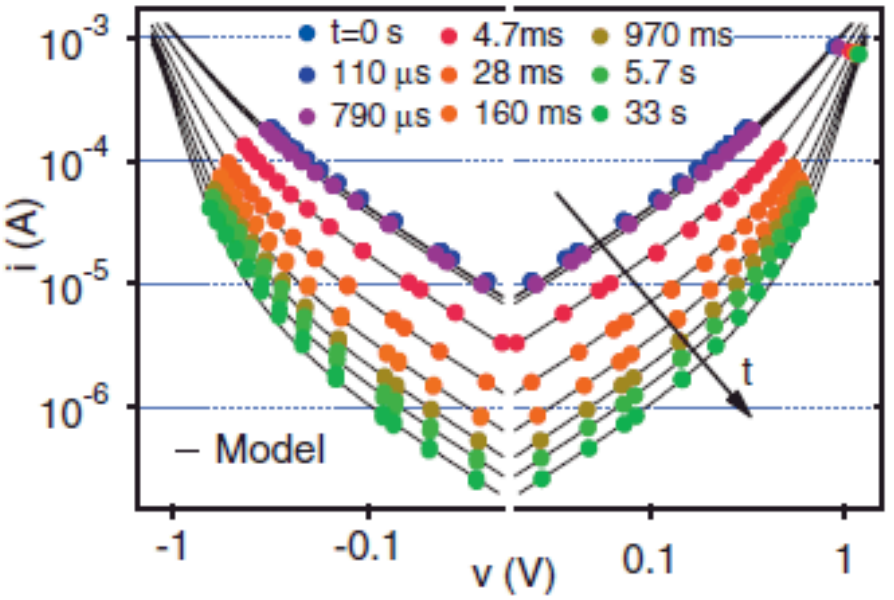
- HP has developed a good model of the TiO_2 memristor
- Represented as a MIM capacitor in series with a resistor
- *w* is the state variable

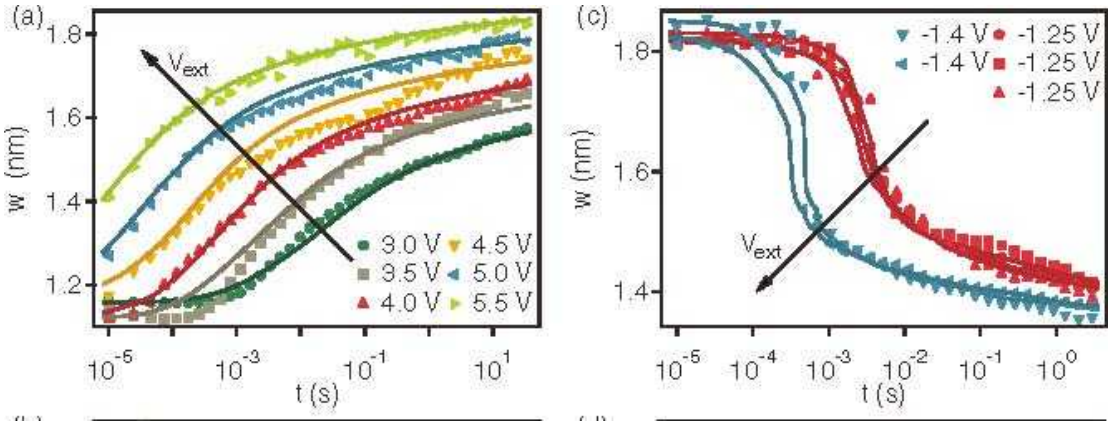


Dynamics of the HP Memristor

- **Capable of many states**

$$\dot{w} = f_{\text{off}} \sinh\left(\frac{i}{i_{\text{off}}}\right) \exp\left[-\exp\left(\frac{w - a_{\text{off}}}{w_c} - \frac{|i|}{b}\right) - \frac{w}{w_c}\right]$$

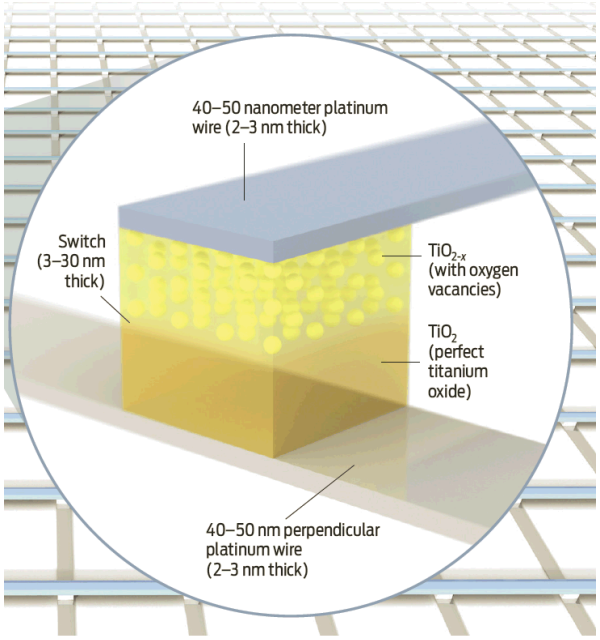


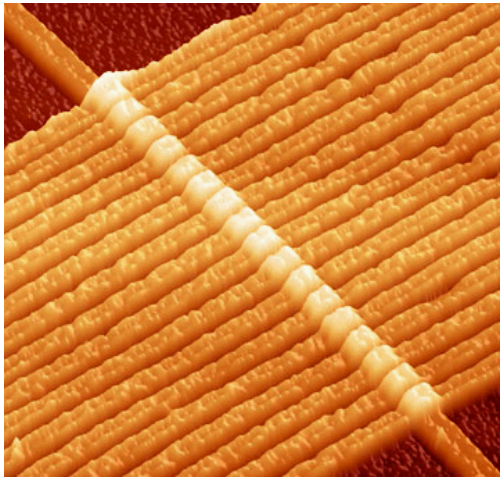


M. Picket t et al, J. Appl. Phys, 106, 74508, 2009.

Memristor Crossbar

- The brain has 10^{10} synapses per cm^2!
- HP (and others) have demonstrated memristors and redox memories in the F = 10-20 nm range
- If we achieve a $1F^2$ device area, density = 10^{12} per cm^2
- Crossbar can be integrated on CMOS transistors
- Back end of line (BEOL) process

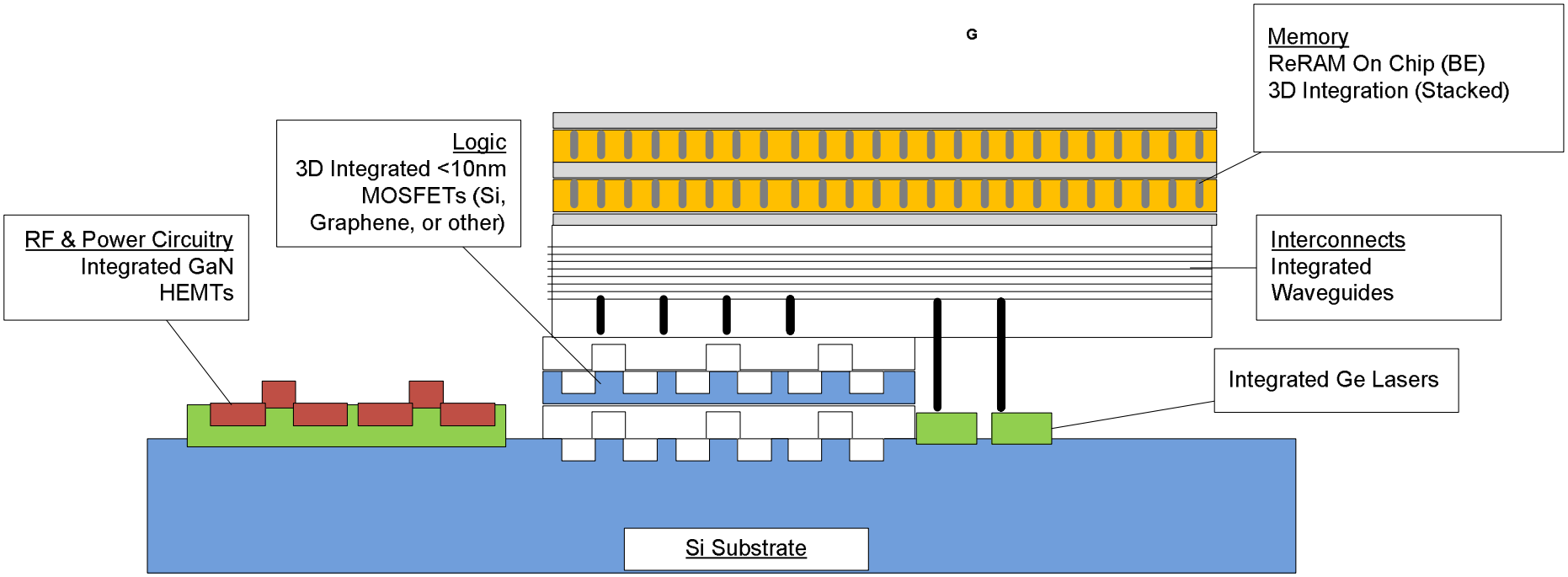




Williams et al, IEEE Spectrum 45, 28, 2008.

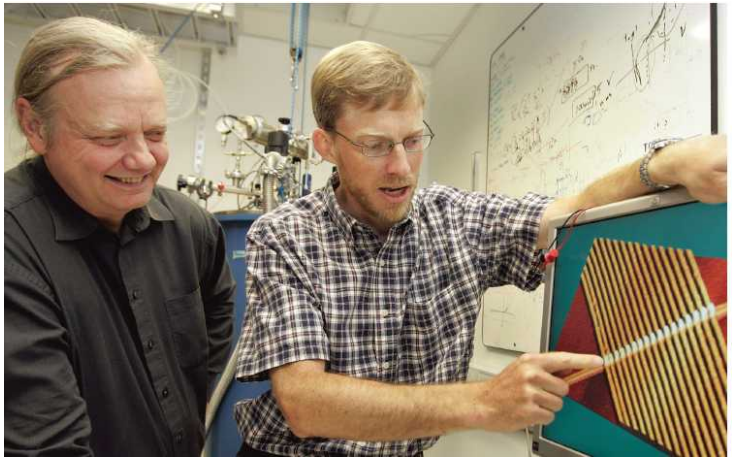
Overall Goal
End of Moore's Law

- **Computer chips of the future will have traditional MOSFETs integrated with memory, optical interconnects, and RF Power circuitry**
- **Memristive (or Redox) memory may have a role**



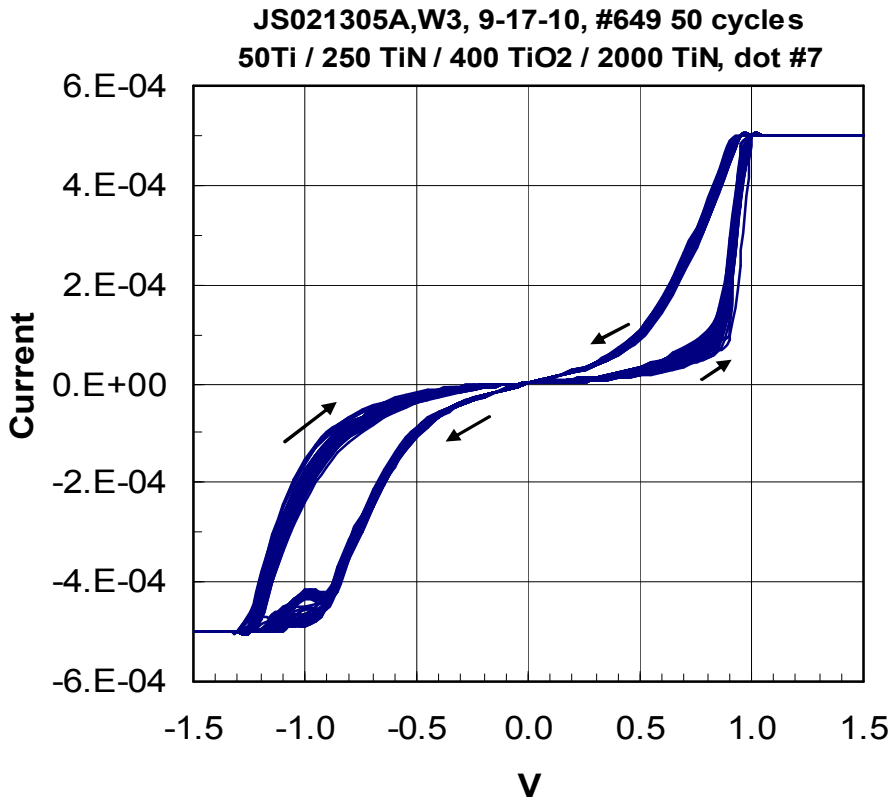
Sandia/HP Collaboration

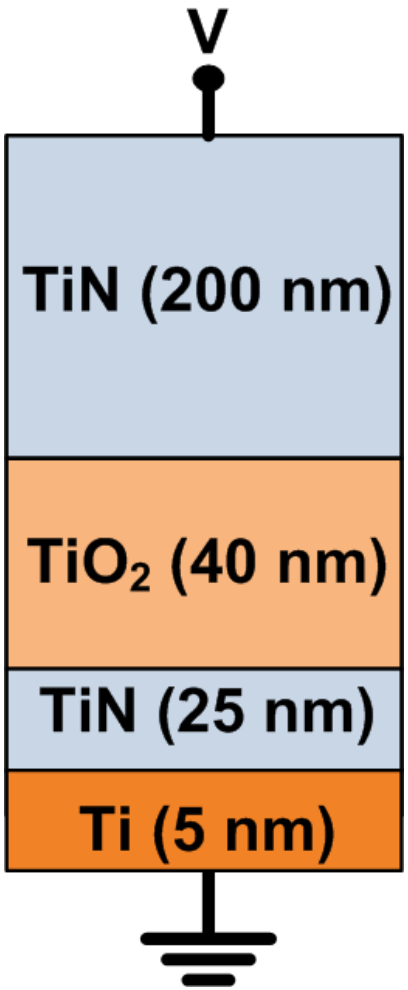
- HP Labs has an integrated memristor/CMOS technology
- Recently we have started a collaboration to transfer this technology in to Sandia (CRADA in progress)
- Several advantages:
  - Capability of creating advanced hardware: hybrid memristor/CMOS chips
  - Neuromorphic hardware integrated on a single chip
- Invitation: Stan Williams will be talking about memristors on March 30th at Sandia

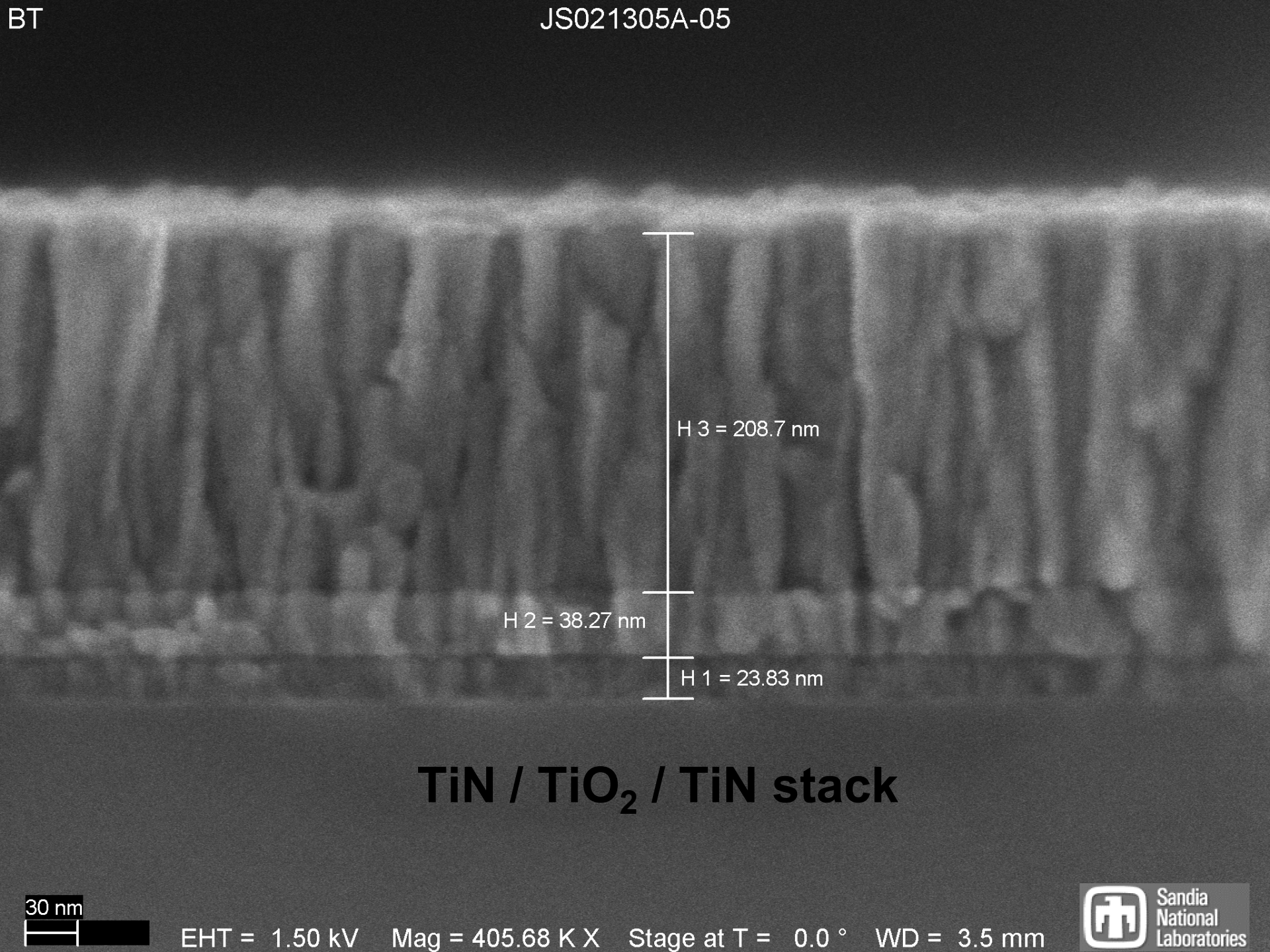


Sandia Memristors

- We are early in our fabrication work
- Have created memristors from several materials (one never before used)
- Collaborations are forming to create state of the art devices

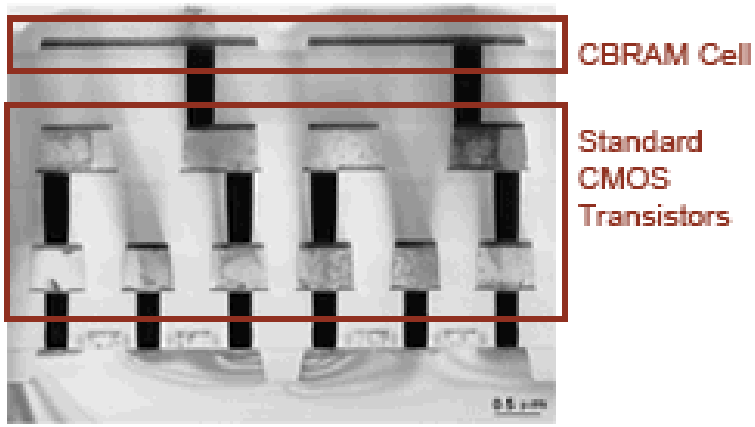





BT
JS021305A-05
H 3 = 208.7 nm
H 2 = 38.27 nm
H 1 = 23.83 nm
TiN / TiO2 / TiN stack
30 nm
EHT = 1.50 kV
Mag = 405.68 K X
Stage at T = 0.0 °
WD = 3.5 mm
Sandia National Laboratories

Programmable Metallization Cell

- The original two terminal memristive device
- Invented by Michael Kozicki, ASU (currently on sabbatical as Chief Scientist of Adesto, Founder of ASU Spinoff Axon Tech)
- Adesto is developing CBRAM as a flash memory replacement – they are quite far along
- Sandia is pursuing a relationship with Adesto

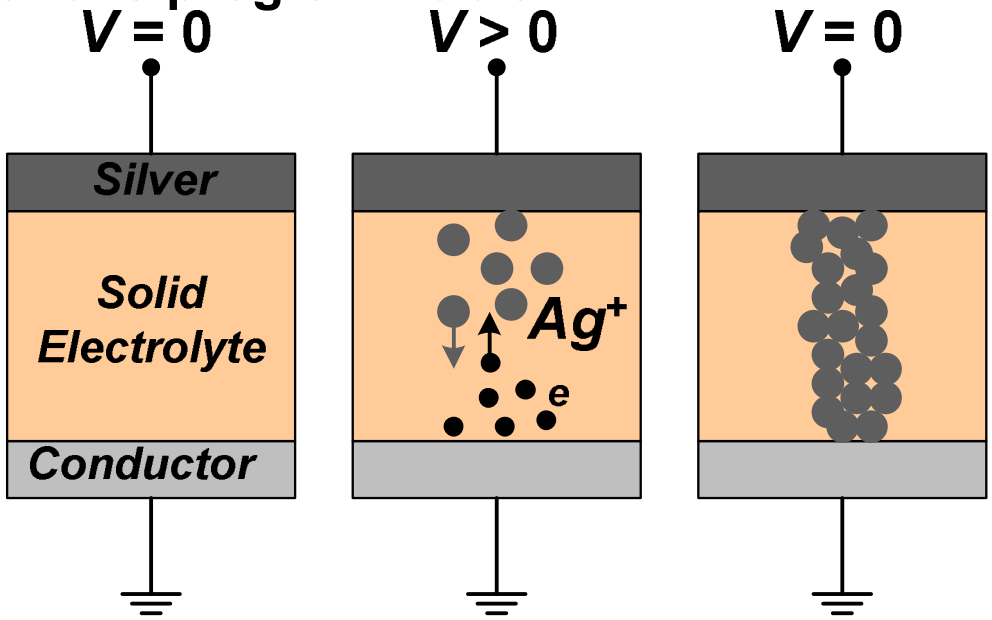


http://www.adestotech.com

http://www.axontc.com

Programmable Metallization Cell

- Ions move under the influence of an electric field leading to *electrochemical reactions*
- Electrochemistry takes place at a few 100 mV
- The electro deposition process stops when a conducting link is formed
- Metallic link reduces the resistance of the structure by many orders of magnitude
- *On* resistance is determined by the programming current and is programmable



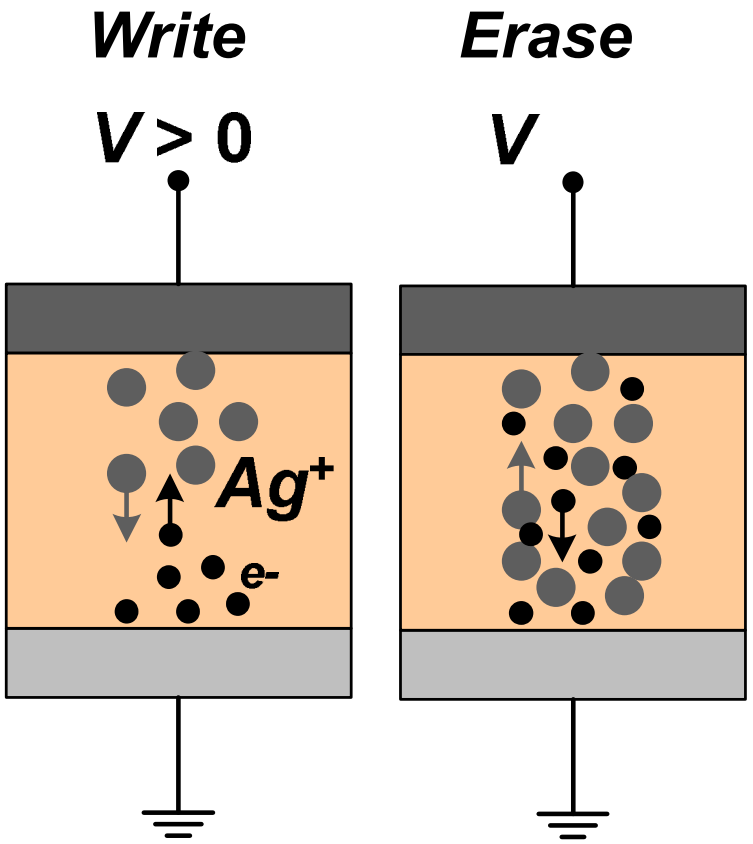
Programmable Metallization Cell

Write

- Low voltage injects silver ions into the electrolyte
- Ions are reduced by the electron current to form stable silver atoms
- Information is stored by the presence of excess silver
- Multiple levels possible

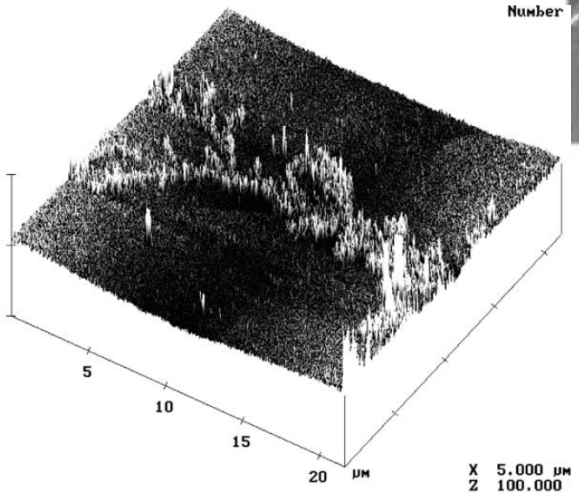
Erase

- A very small reverse voltage (a few hundred mV) removes excess silver from the electrolyte
- Device is easily erased
- Excess silver is replaced on the silver electrode in an easily reversible reaction

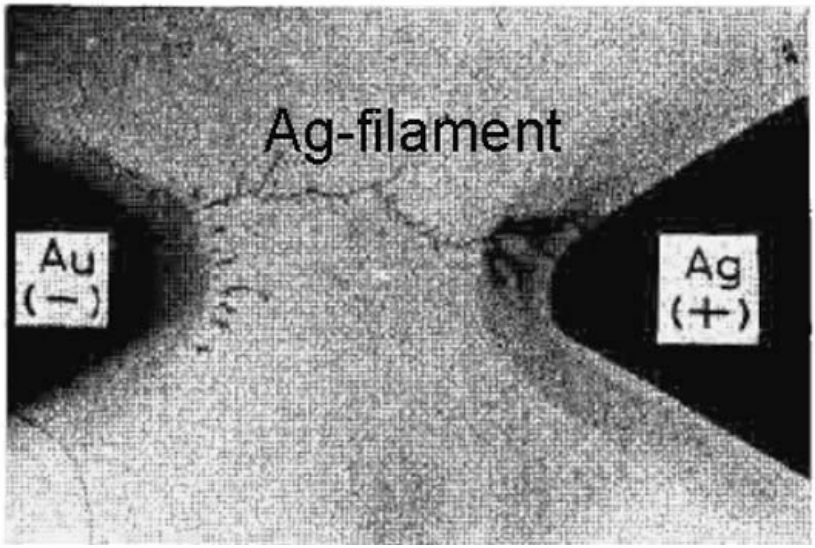


Programmable Metallization Cell

- **Metallization looks like a dendrite**



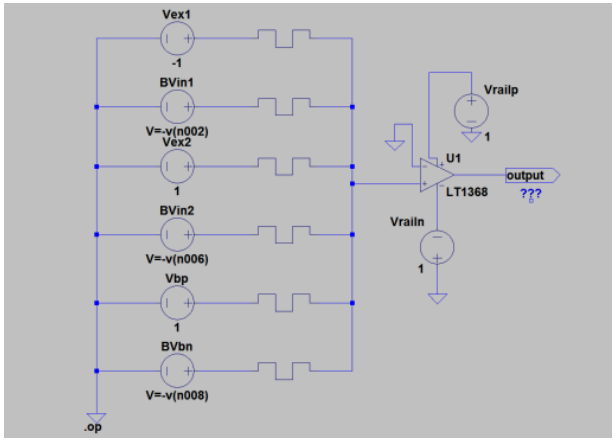
M.N. Kozicki et al. , Physica E 19 , 161, 2003

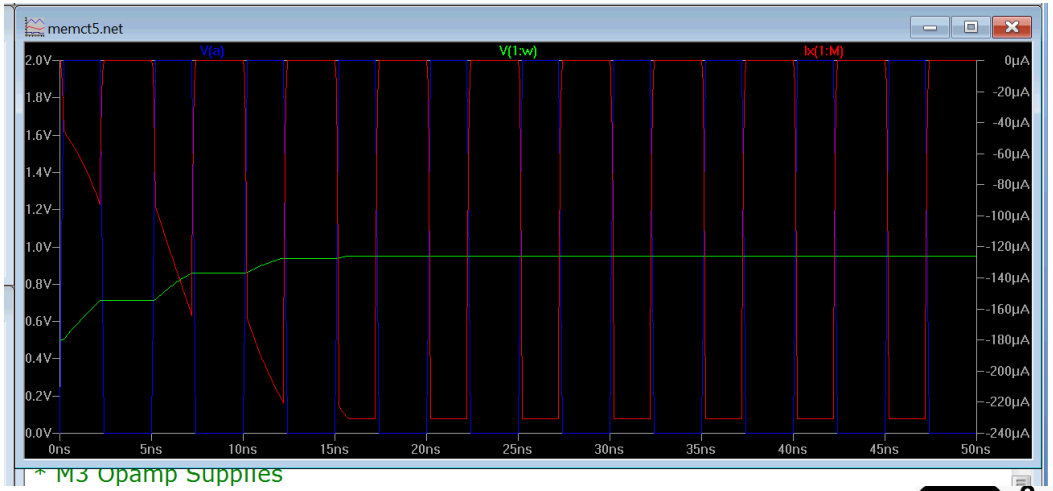


Y. Hirose, J. Appl. Phys.. 47, 2767, 1976.

SPICE Modeling

- SPICE allows simulation of neuromorphic circuits
- Sandia has extensive SPICE capabilities to simulate neuro
- Current Sandia SPICE Model
  - Simplified SPICE model by Lehtonen and Laiho
  - Converting to HP Lab's Pickett model



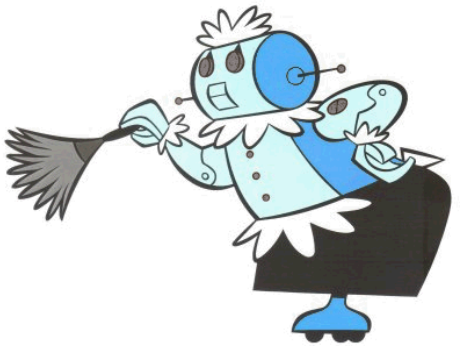


Part III: Neuromorphic Computing with Memristors

Why Neuromorphic Computing?

- **Why do we bother studying neuromorphic computing?**

1. **Exascale computing: The brain is much more efficient than current supercomputers – especially for certain applications**
2. **As the semiconductor industry confronts the end of Moore's law, we are starting to take great interest in new devices and architectures that may continue to increase the performance and intelligence of computer chips**
3. **Deal with "crummy" devices**
4. **Smart robotic butlers?**



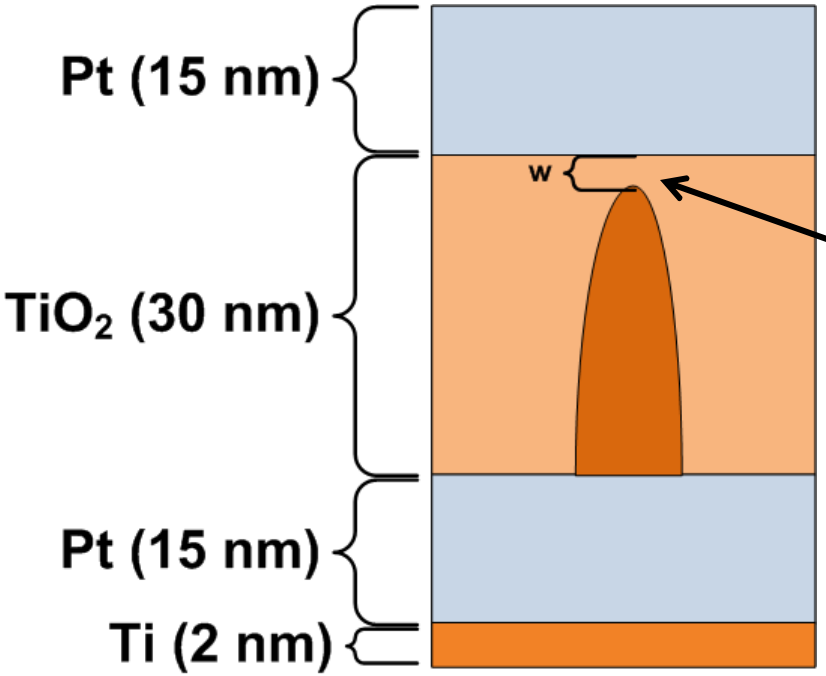
Why Neuromorhpic Computing?

- Cray XT5 Jaguar (ORNL), hex-core
- ~2×10^{15} flops/s, ~10 MW, room-sized
- ~100 Gbits/in^2
- access-limited (processor disconnected from memory)

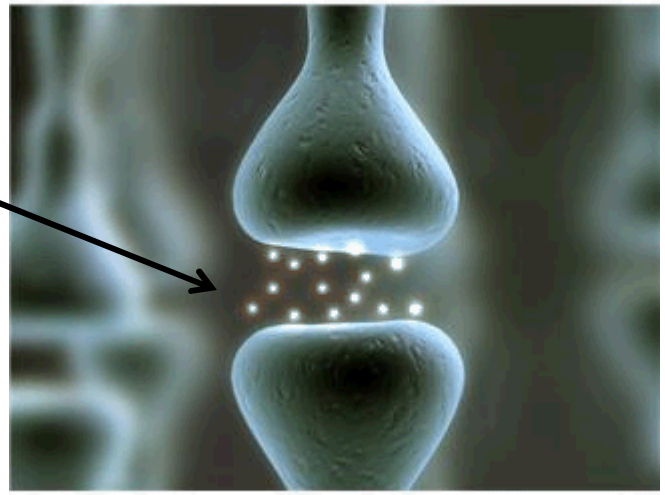
- Brain, 10^{11} neurons, 10^{15} glial cells
- >10^{16} flops/s, 20W, 1200 cm^3
- ~infinite memory storage capacity?
- near instant memory access

Why Memristors?

- To quickly review, the memristor is an electrical synapse
- Synaptic weight = memristor state



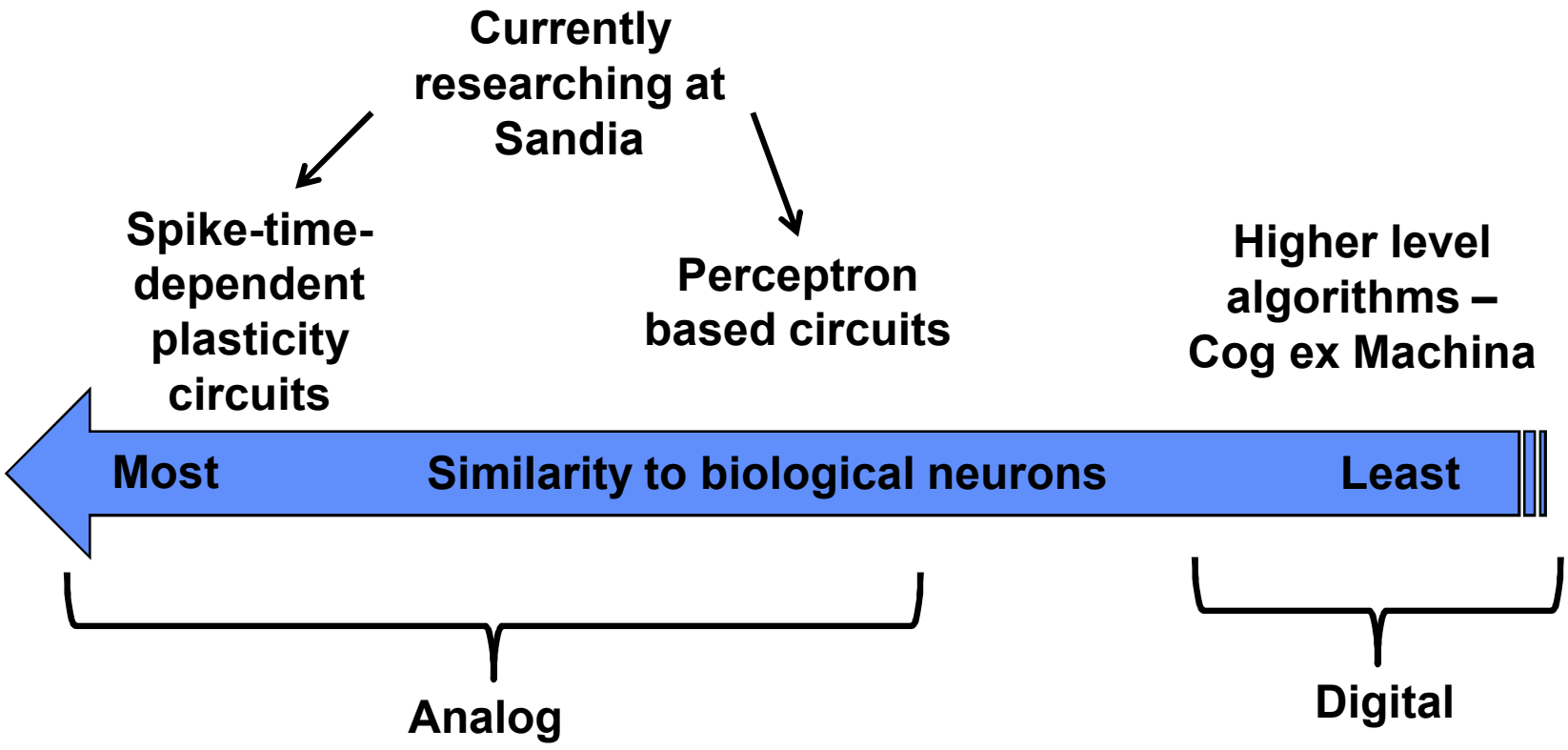
memory



wikipedia.org

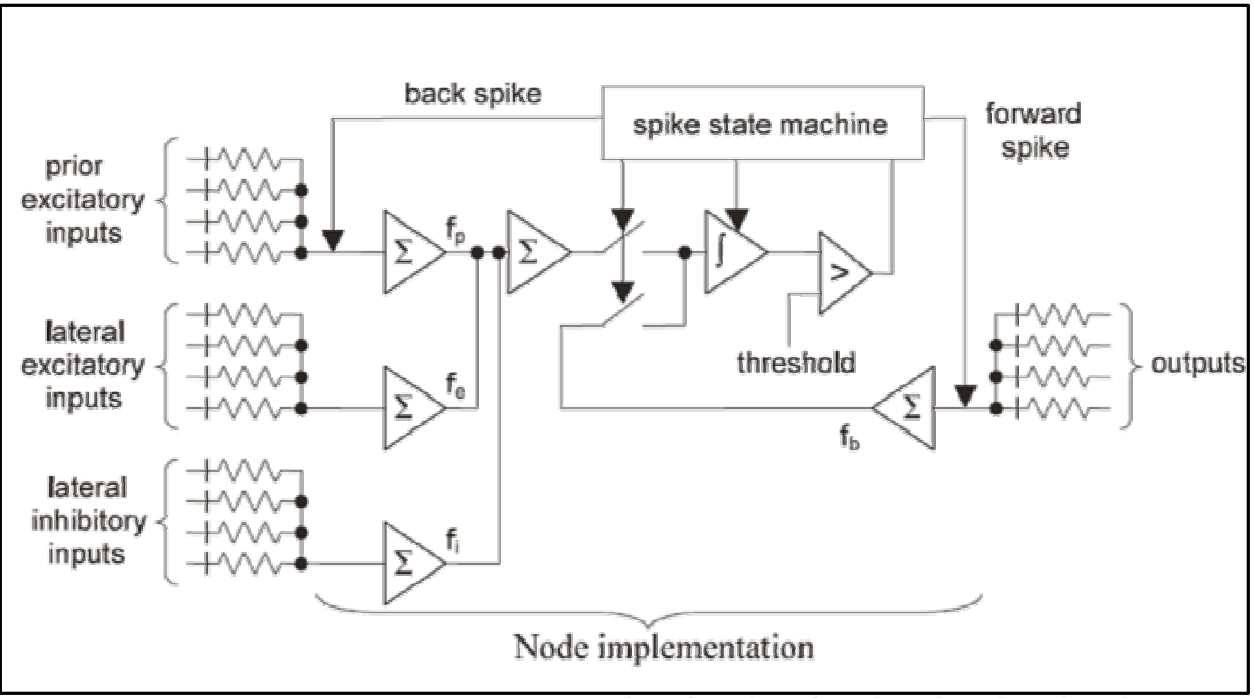
Neuromorhpic Computing with Memristors

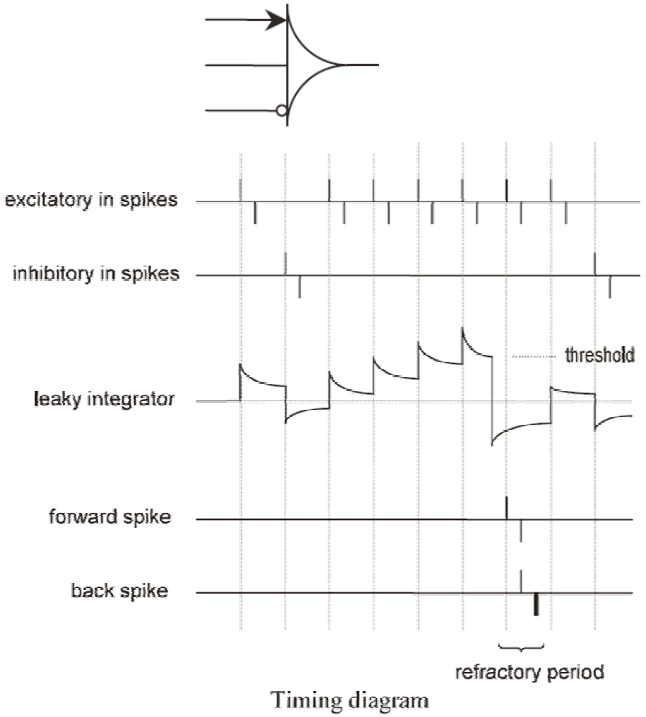
- More than one way to skin a cat



Spike Time Dependent Plasticity

- The most biological approach
- Forward and backward spikes
- Currently being researched by several groups including Sandia
- STDP with memristors pioneered by Greg Snider, HP Labs

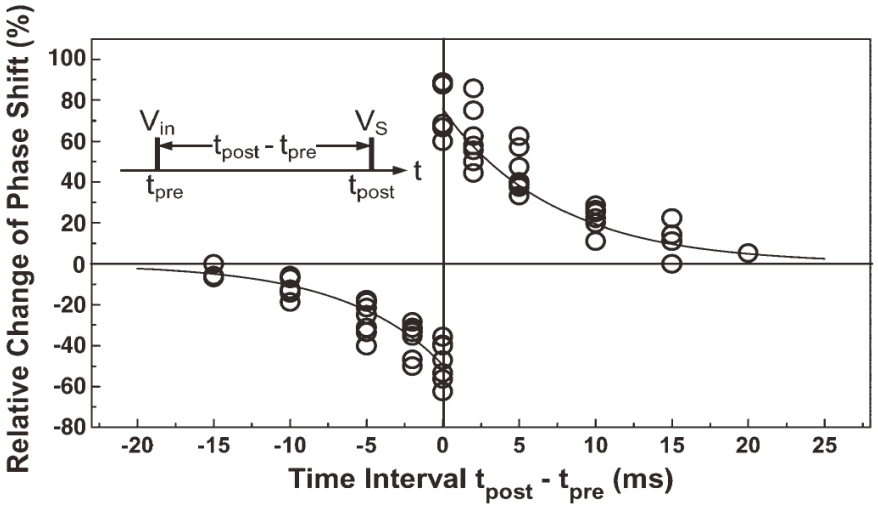




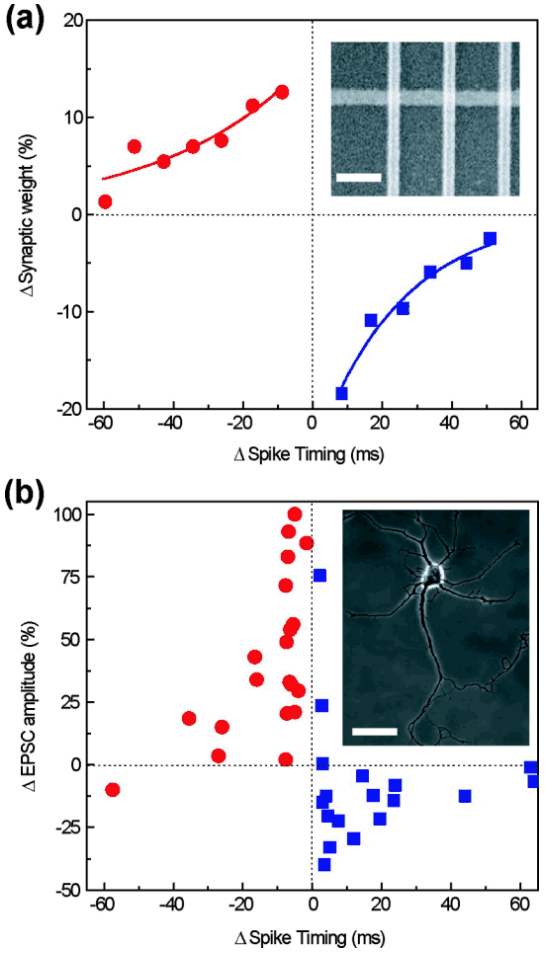
G.S. Snider, Nanotechnology, 18, 365202, 2007.

Spike Time Dependent Plasticity

- **STDP has been demonstrated experimentally with memristors by groups at U. Michigan and UCLA**



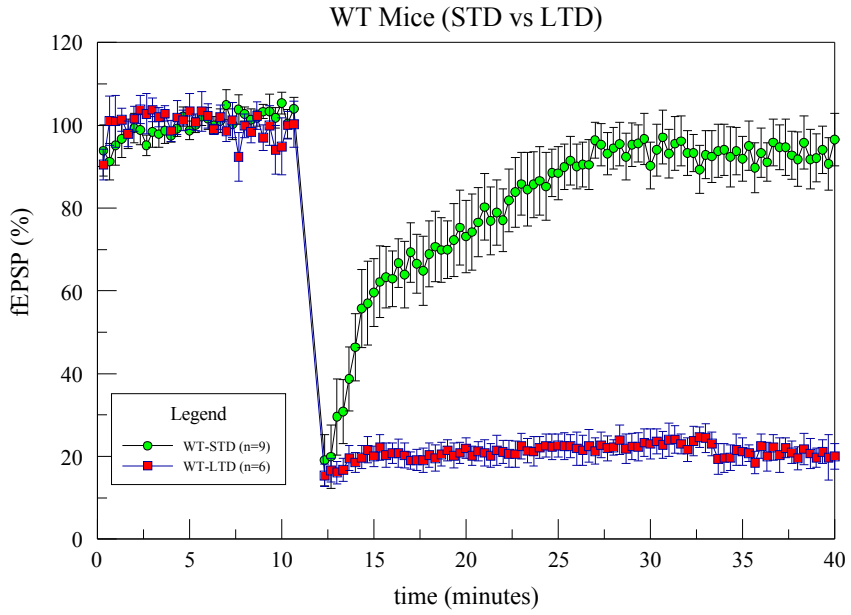
L. Zhang et al, IEEE Electron Dev Lett, 31, 716, 2010.



S.H. Jo et al, Nano Lett, 10, 1297, 2010.

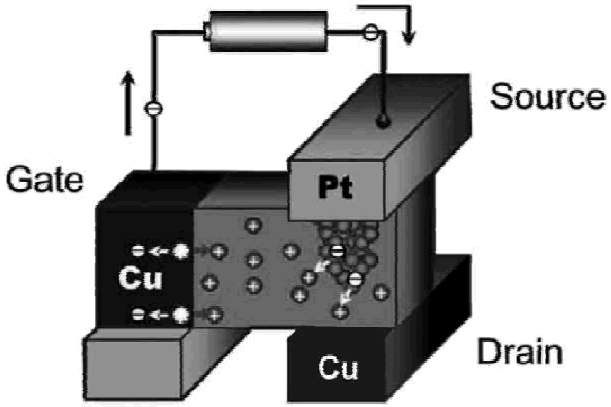
Moving Closer to Biology

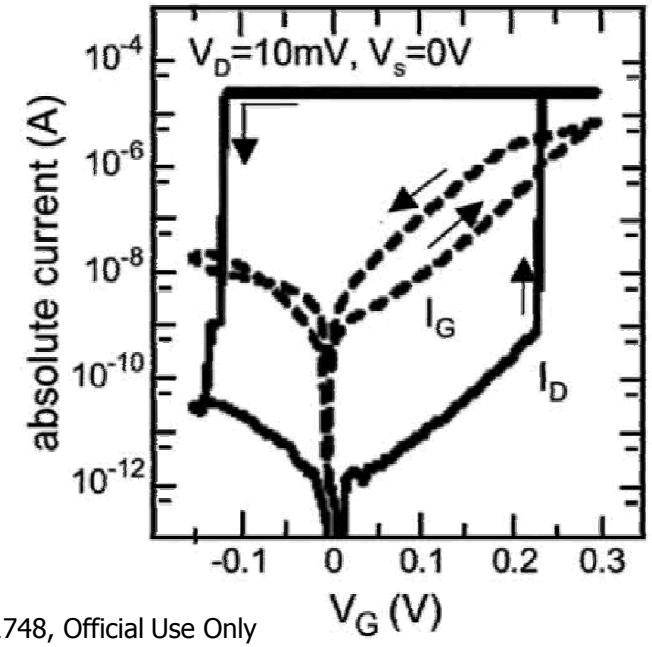
- **New Sandia Project – create neuromorphic circuits that mimic biological processes such as:**
  - **Long term depression (LTD)**
  - **Short term depression (STD)**
- **Caused by high frequency stimulation (> 100 Hz)**
- **Unknown origin, but molecular mechanisms have been hypothesized**



Moving Closer to Biology

- Goal: Neuromorphic circuits that regulate computation and storage of info in memristor structures
- Optical methods?
- Atomic Switch – Control the resistance change
  - Three terminal memristive device
  - Pioneered by Masakazu Aono (NIMS)
  - Filament formation controlled by gate





Aono et al, Proc. IEEE,, 98 2228, 2010.

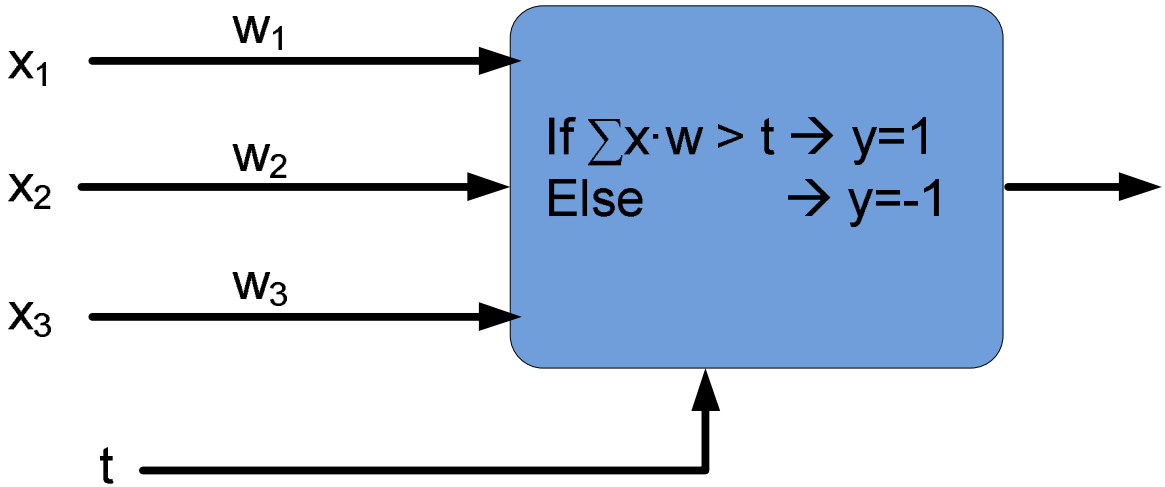
STDP and Highly Biological Methods

- **Status of STDP and STD/LTD Biologically Inspired Hardware Research at Sandia**
  - **PI: Conrad James**
  - **Currently studying frequency/time dependence of STD/LTD (with rat brain tissue)**
  - **Next Phase: develop hardware to mimic biology**
- **Advantages of STDP and highly biological approaches**
  - **May be most efficient method of computation**
  - **Nature gives proof of concept**
- **Disadvantage - Requires analog time dependent use of memristor**
  - **Difficulty implementing open loop**
  - **Complexity implementing closed loop**
  - **Timing difficulties**

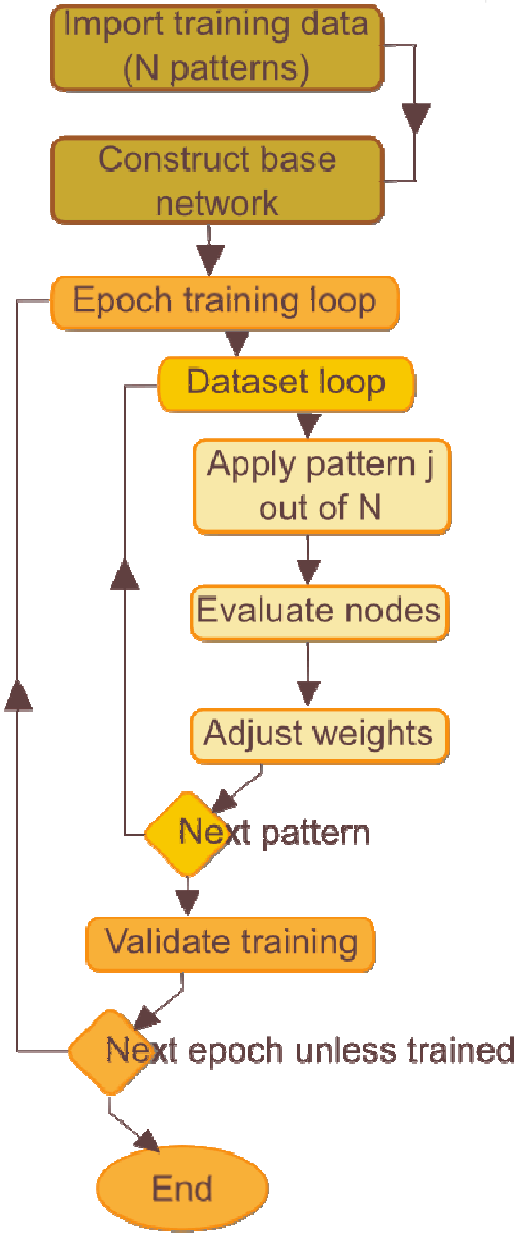
Perceptron Based Neural Nets

- Perceptron is the simplest model of a neuron
- Feed forward network
- Single node can learn linearly separable logic functions
- Applications:
  - Field programmable gate arrays
  - Pattern recognition

< 0

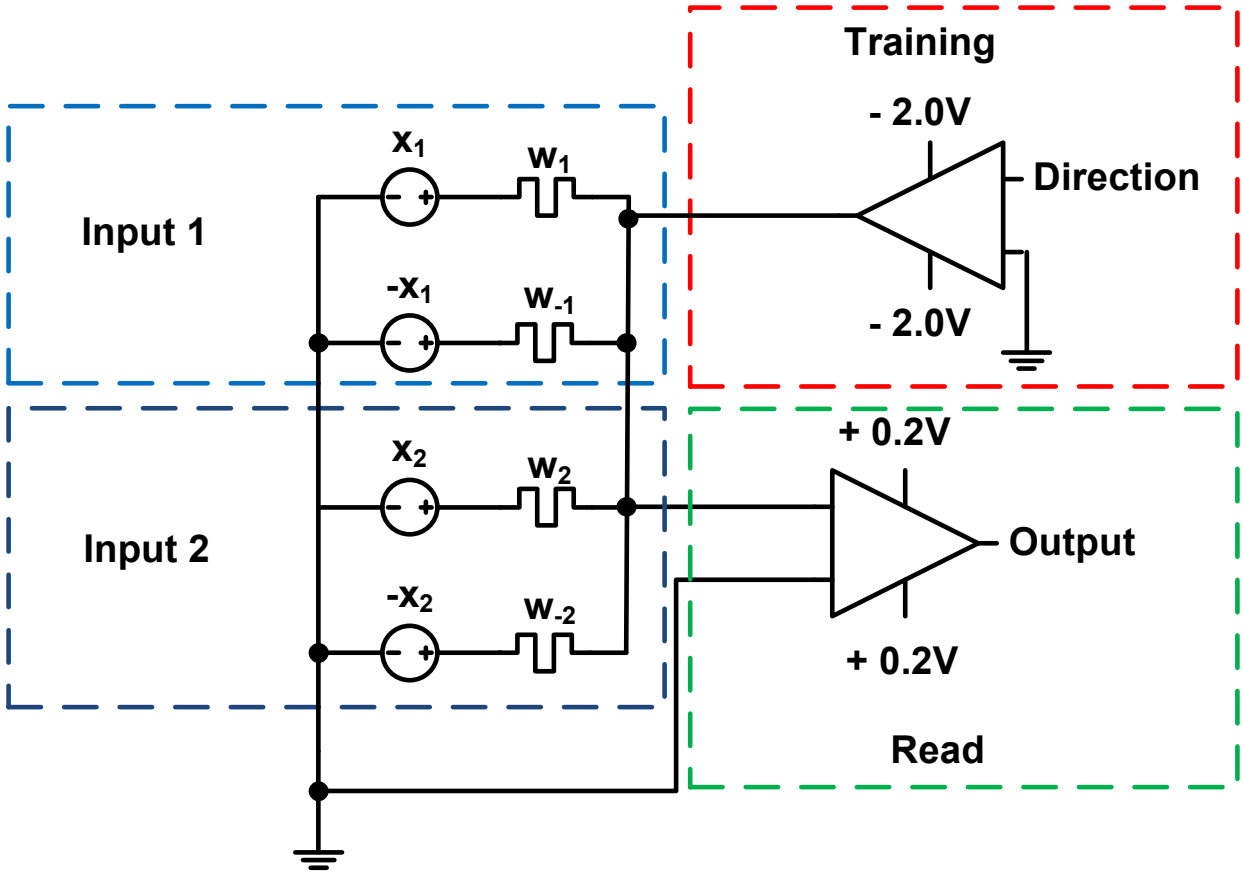


Algorithm (Simplified)



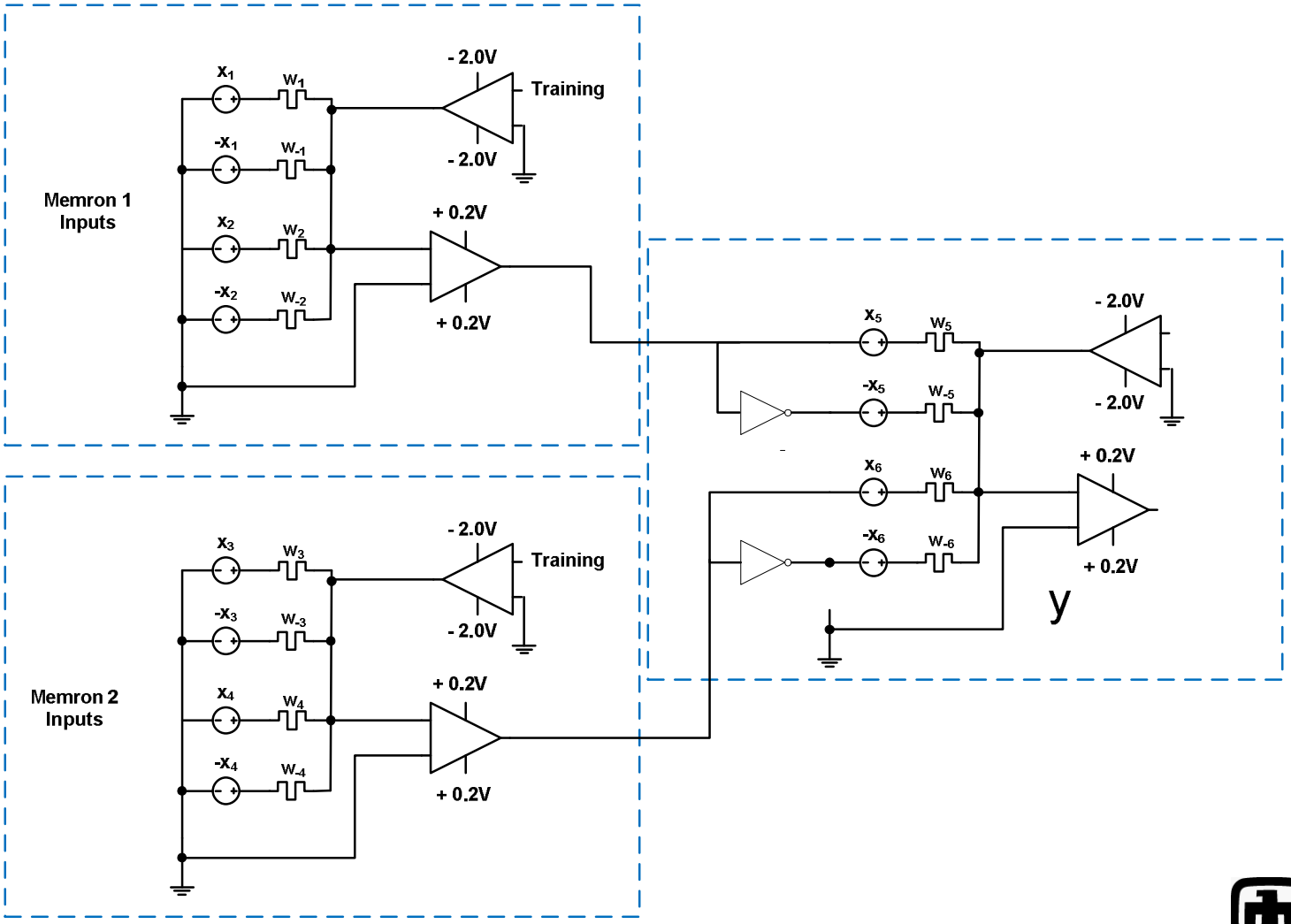
Memron

- We translated the neuron to hardware using memristors
- We have a working model that uses LTSpice and C++



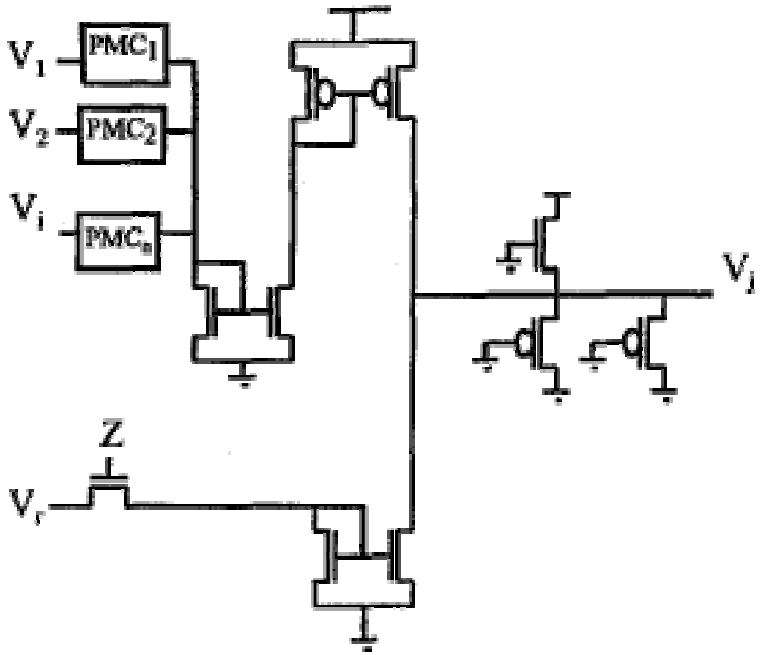
Memron

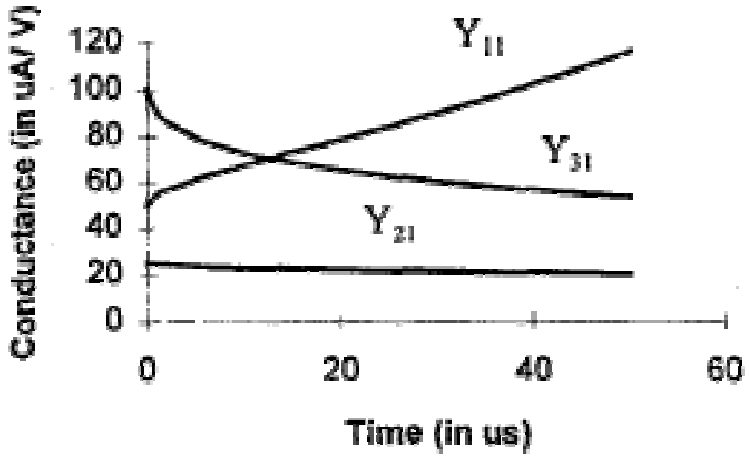
- **Requires 3 Memrons to learn XOR:**



Early Work

- Research by Michael Kozicki's group at ASU in 1998
- Possibly the earliest research using a two terminal memristive device to implement an electronic neural network





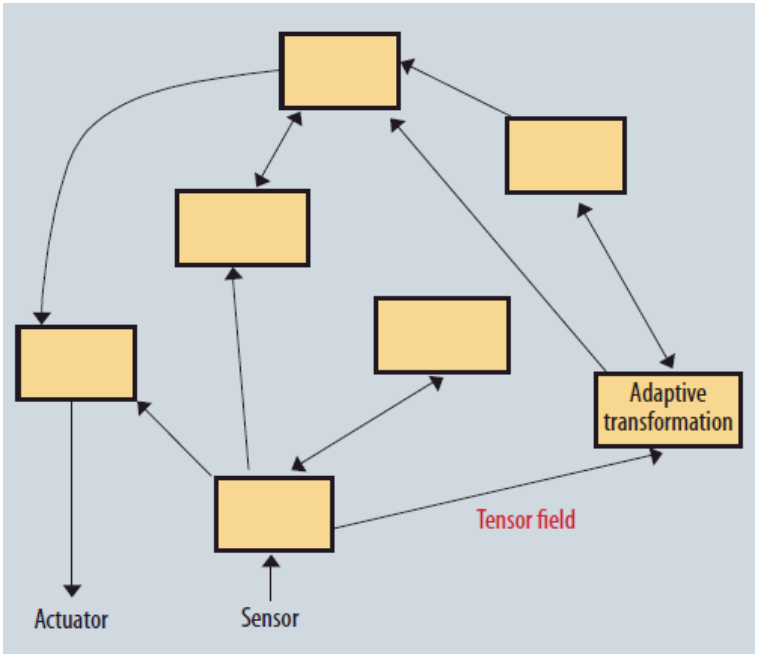
Swaroop et al, ISCAS 98, 33, 1998.

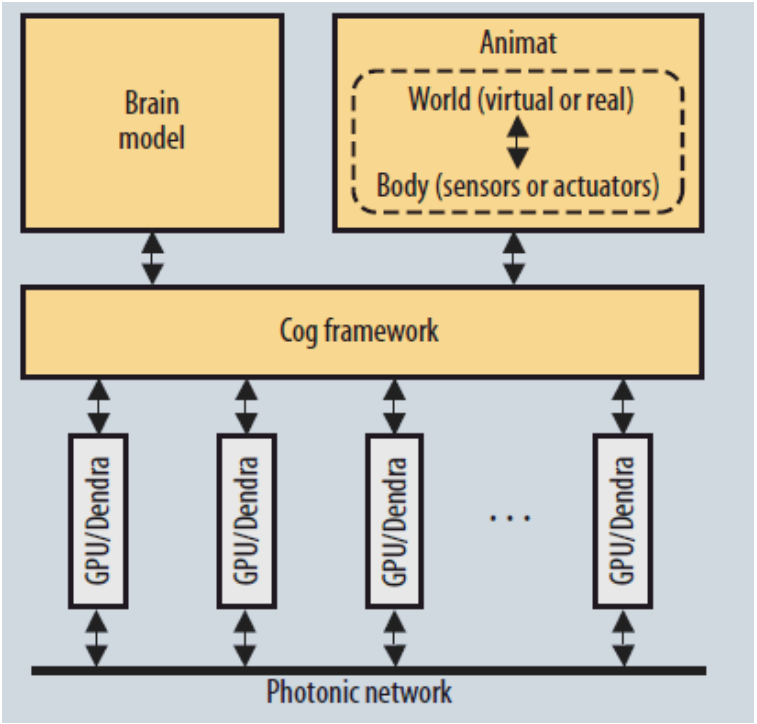
Memron

- Status of "Memron" Research at Sandia
  - Algorithm fully implemented in software (in debug and optimization phase)
  - Read algorithm implemented in SPICE
  - Currently designing the training algorithm
- Advantages
  - Much simpler than STDP
  - Simple circuitry and architecture
  - Easier to implement in hardware
- Disadvantages
  - Requires analog use of memristor
  - Simplicity could limit robustness

Cog ex Machina

- Recently developed by Greg Snider at HP Labs
- Emerging software based neuromorphic architecture
- Uses tensors and mathematical "tricks" to solve problems
- Hypothesis: STDP is not necessary to implement neuromorphic processing

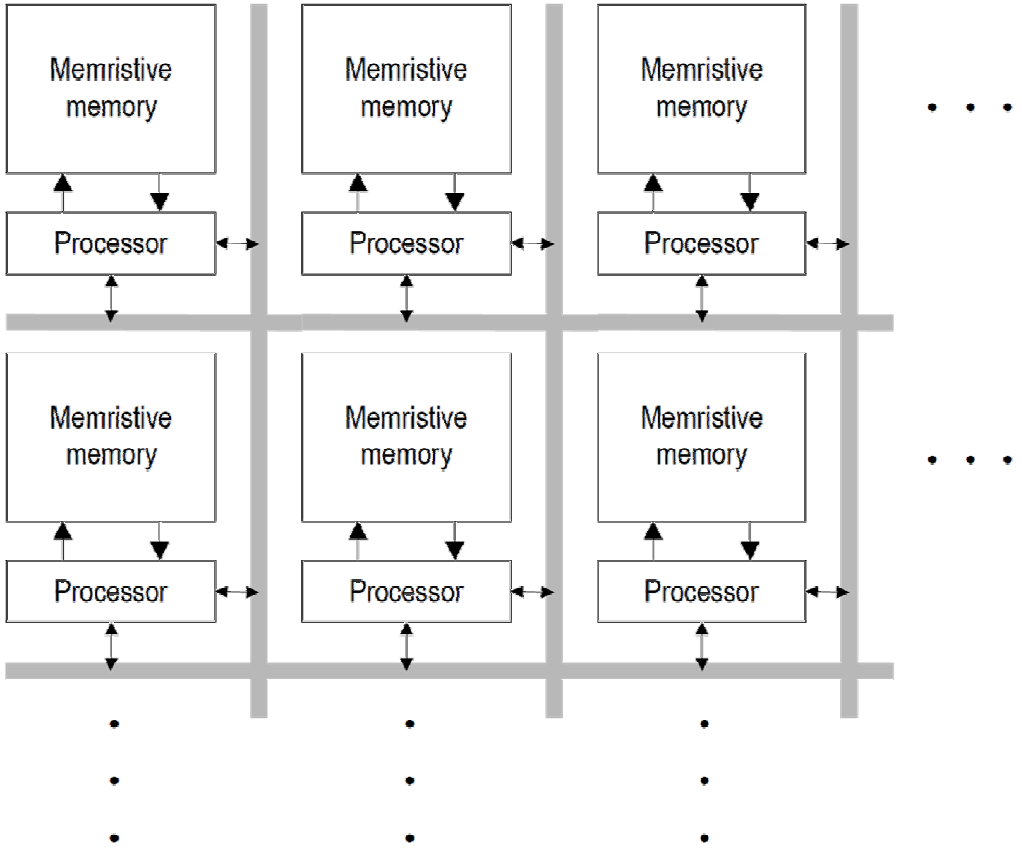




G.S. Snider, Computer, 44, 21, 2011.

Cog ex Machina

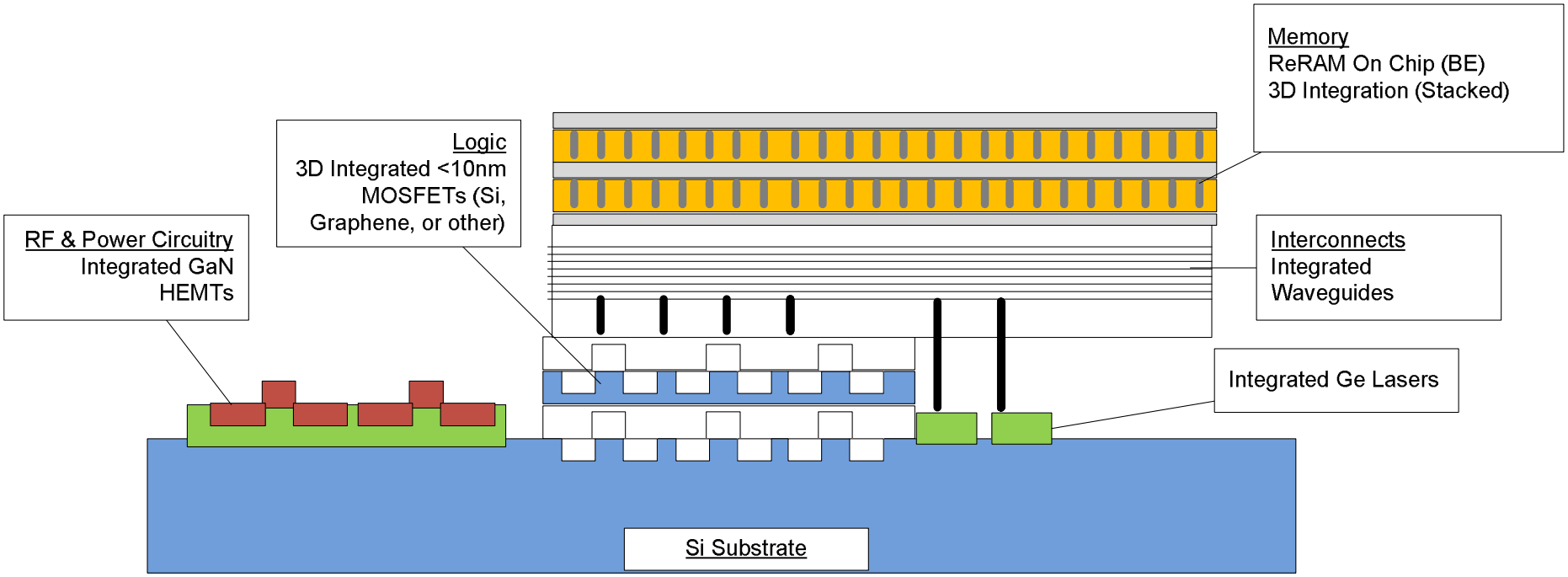
- **Uses high performance on chip memory – such as memristors**
- **Multiple processor cores required**



G.S. Snider, Computer, 44, 21, 2011.
Matt Marinella, Org 1748

Cog ex Machina fits well with Computer Chips of the Future

- **Computer chips of the future will have traditional MOSFETs integrated with memory, optical interconnects, and RF Power circuitry**
- **Memristive (or Redox) memory may have a role**



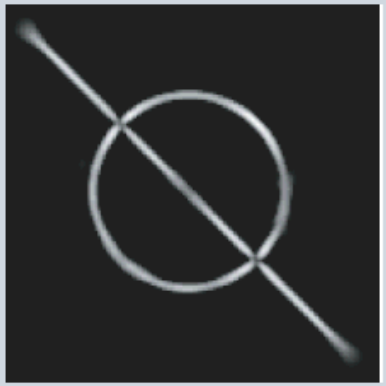
Cog ex Machina

- Contrast normalization (left)
- Boundary completion (right)

(a)

(b)

(a)



(b)

G.S. Snider, Computer, 44, 21, 2011.

Cog ex Machina

- Status
  - Greg Snider and HPL Team have recently demonstrated algorithm with GPU simulations
  - Sandia was not involved in this development
  - Very promising - we are currently learning more about it
  - Greg recently visited us and we are exploring collaborative opportunities
- Advantages
  - Cleverly makes uses of future commercial technology
  - Does not require analog memristive memory
  - Demonstrated ability to “learn” and solve complex problems already
- Disadvantages
  - Hardware not yet available (5 or more years out)
  - Not biological at a low level

Summary of Memristor Based Neuropmorphic Research at Sandia

- Memristor Technology Development
  - Goal: Create an integrated CMOS/memristor platform
  - Contacts: Matt Marinella, Jim Stevens, Tom Zipperian
- Memron Algorithm Development
  - Goal: Create a working learning circuit
  - Contacts: Matt Marinella, Alex Hsia
- Spike Time Dependent Plasticity with Memristors
  - Goal: Demonstrate STDP and LTD/STD with memristor circuits
  - People: Conrad James (neuroscience), Matt Marinella (memristor technology)
- Note: several other memristor projects also

Summary and Future Outlook

- Sandia has extensive microfabrication and device capabilities, and a strong cognitive science program
- Recently formed collaboration intends to demonstrate biologically inspired neuromorphic hardware
- The memristor is a novel two terminal device with synapse-like behavior
- May be a critical component for neuromorphic systems
- There are a range of methods to use the memristor to create neuromorphic systems
  - Very biological – STDP
  - Somewhat biological – Perceptron/Memron
  - System level – Cog ex Machina
- Sandia is forming a collaboration with HP to design and fabricate state of the art memristor structures
- We are interested in collaborations!

Acknowledgements/Info

- Would like to acknowledge useful discussions with Greg Snider, Stan Williams and the HP Labs Memristor Research Team, and Michael Kozicki
- Funding provided by Sandia's Laboratory Directed Research and Development (LDRD)

- Invitation: Stan Williams will be talking about memristors on March 30th at Sandia (see me after for more info)
- Contacts for Additional Info:
  - LTD/STD, STDP with Memristors: Conrad James, cdjame@sandia.gov
  - Cog ex Machina: Greg Snider, snider.greg@hp.com
  - Programmable Metallization Cell: Michael Kozicki, michael.kozicki@asu.edu

Questions???

- ***Macy Violet Marinella, Born February 19, 2011***

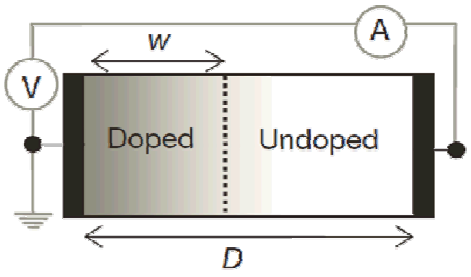
Thanks!

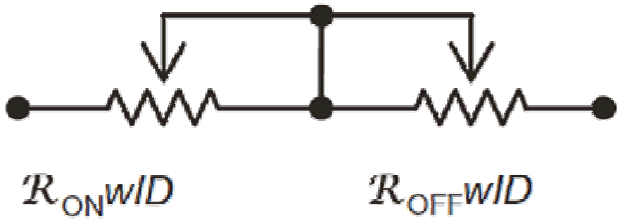
- ***DARPA's stated goal is a brain that works "at the cat level" and fits in a two-liter soda bottle***

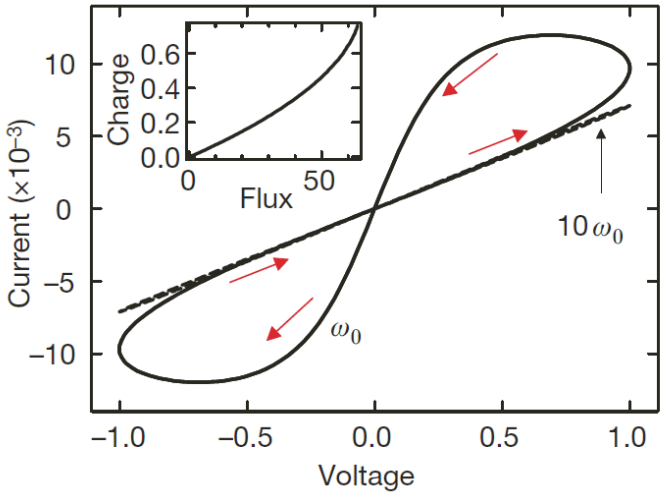
http://www.popsci.com/technology/article/2010-04/darpa-dreams-electronic-cat-brains-based-memristors

Memristor Model

- **HP's original two resistor ("toy") model*:**

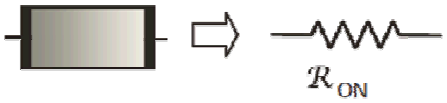






Undoped:

Doped:



$$v(t) = \left(\mathcal{R}_{ON}\frac{w(t)}{D} + \mathcal{R}_{OFF}\left(1 - \frac{w(t)}{D}\right)\right) i(t)$$

$$\frac{dw(t)}{dt} = \mu_V \frac{\mathcal{R}_{ON}}{D} i(t)$$

$$w(t) = \mu_V \frac{\mathcal{R}_{ON}}{D} q(t)$$

*This "toy" model is still the basis of many SPICE models derived in the literature

Strukov et al, Nature 459, 1154, 2009.

What is Memristor?

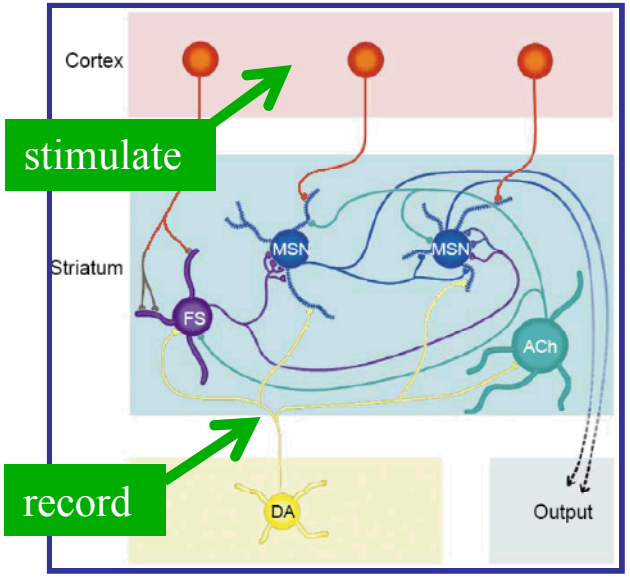
Leon Chua, father of the memristor

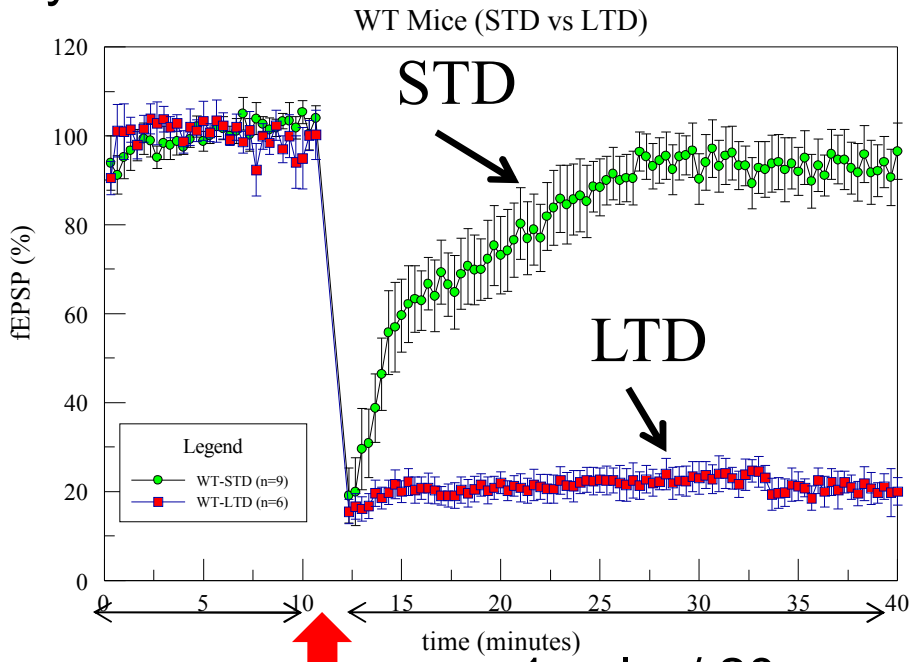
From the circuit-theoretic point of view, the three basic two-terminal circuit elements are defined in terms of a *relationship* between two of the four fundamental circuit variables, namely, the *current* i, the *voltage* v, the *charge* q, and the *flux-linkage* φ. Out of the *six* possible combinations of these four variables, five have led to well-known relationships [1]. Two of these relationships are already given by $q(t)=\int_{-\infty}^{t} i(\tau)\,d\tau$ and $\varphi(t)=\int_{-\infty}^{t} v(\tau)\,d\tau$. Three other relationships are given, respectively, by the *axiomatic* definition of the three classical circuit elements, namely, the *resistor* (defined by a relationship between v and i), the *inductor* (defined by a relationship between φ and i), and the *capacitor* (defined by a relationship between q and v). Only one relationship remains undefined, the relationship between φ and q. From the logical as well as axiomatic points of view, it is necessary for the sake of *completeness* to postulate the existence of a fourth basic two-terminal circuit element which is characterized by a φ–q curve.[2] This element will hencefortth be called the *memristor* because, as will be shown later, it behaves somewhat like a nonlinear resistor with memory.

L.O. Chua, IEEE Trans Circuit Theory 18, 507, 1971.

More Biological Approach

- Take this research a step further: move closer to biology
- Hypothesis: replicating biological mechanisms of ***information storage and processing*** will increase computing efficiency
- Short-term and long-term depression (STD, LTD) can be induced in the striatum with high-frequency stimuli in the cortex





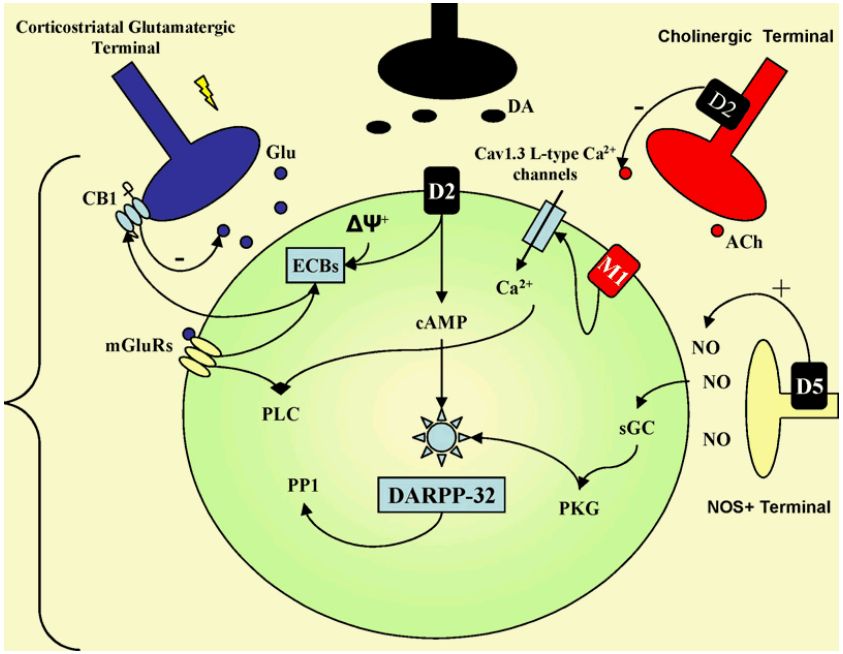
1 pulse/ 20s

1 pulse/ 20s

100 pulses/ 20s

M. Baca, M. Wilson, A. Allen, D. Partridge

Can Biological Mechanisms be Replicated in Hardware?



Synapse function involves bidirectional transport:

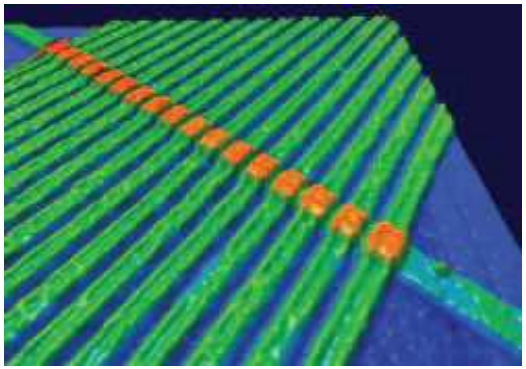
- presynaptic-to-post: Glu, DA, NO
- extracellular-to-postsynaptic: Ca^{2+}
- postsynaptic-to-pre: CB1

Keys to biological computing:

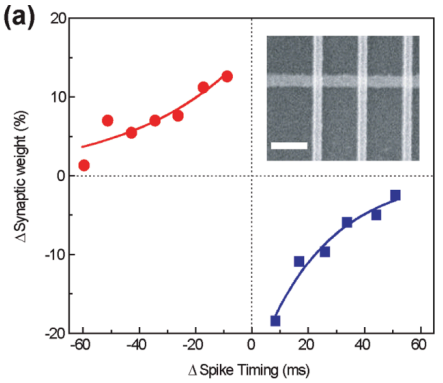
- nanoscale phenomena
- timing/frequency dependence
- multi-scalar phenomena (ms to hours, microns to mm)

Memristor structures:

- compact scaling
- non-volatile
- timing dependent



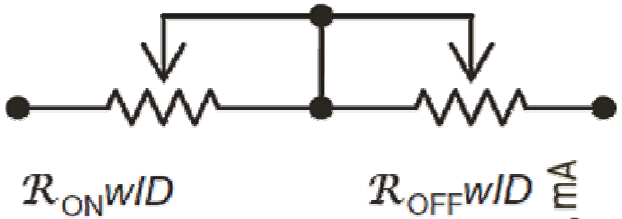
R.S. Williams, IEEE Spectrum , 2008

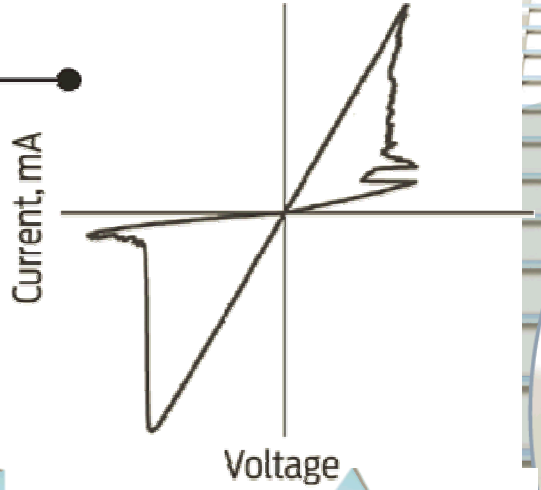


S.H. Jo et al, Nano Lett, 10, 1297, 2010.

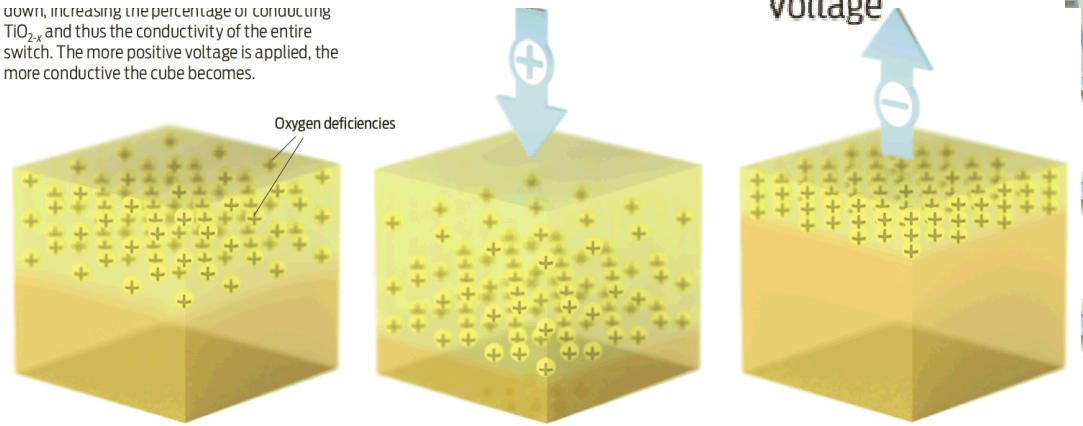
How Does the HP Memristor Work?

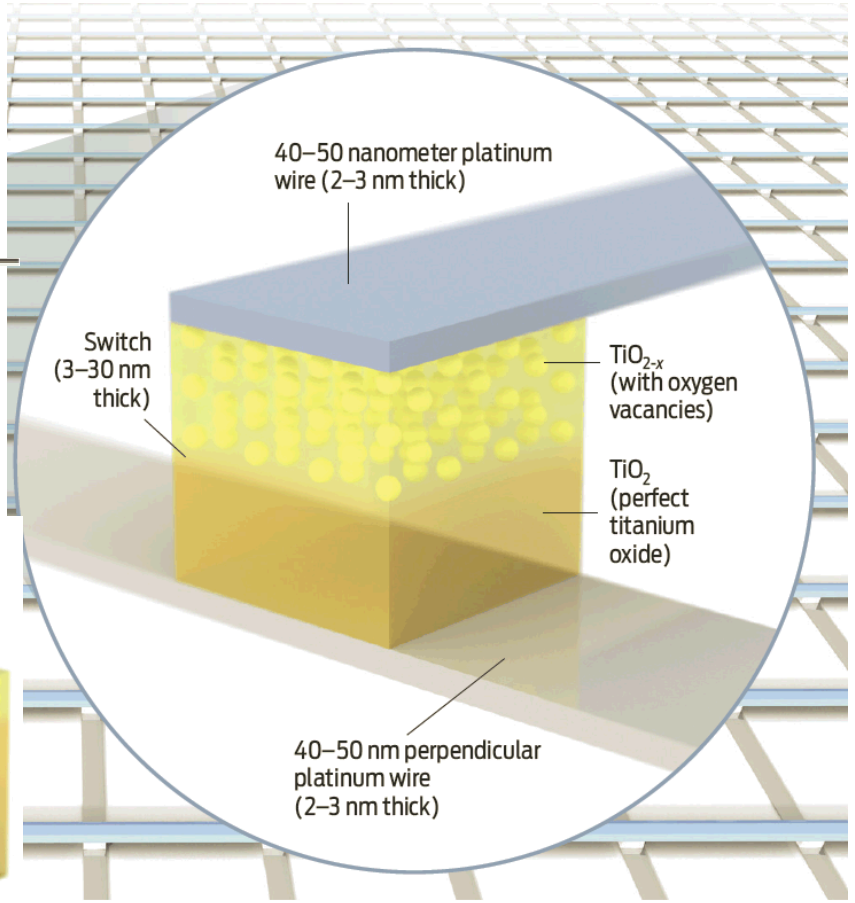
- **A very simple explanation and model:**





down, increasing the percentage of conducting TiO_{2-x} and thus the conductivity of the entire switch. The more positive voltage is applied, the more conductive the cube becomes.





Strukov et al, Nature 459, 1154, 2009. **Williams et al, IEEE Spectrum 45, 28, 2008.**